SPI/I²C Compatible, Temperature Sensor, 4-Channel ADC and Quad Voltage Output DAC

ADT7518

FEATURES

Four 8-bit DACs
Buffered voltage output
Guaranteed monotonic by design over all codes
10-bit temperature-to-digital converter
10-bit 4-channel ADC
  DC input bandwidth
  Input range: 0 V to 2.25 V
Temperature range: –40°C to +120°C
Temperature sensor accuracy of typ: ±0.5°C
Supply range: 2.7 V to 5.5 V
DAC output range: 0 V to 2 V_{REF}
Power-down current: 1 µA
Internal 2.25 V_{REF} option
Double-buffered input logic
Buffered reference input
Power-on reset to 0 V DAC output
Simultaneous update of outputs ($\overline{LDAC}$ function)
On-chip rail-to-rail output buffer amplifier
SPI®, I²C®, QSPI™, MICROWIRE™, and DSP-compatible
  4-wire serial interface
SMBus packet error checking (PEC)-compatible
16-lead QSOP package

APPLICATIONS

Portable battery-powered instruments
Personal computers
Smart battery chargers
Telecommunications systems
Electronic text equipment
Domestic appliances
Process control

PIN CONFIGURATION

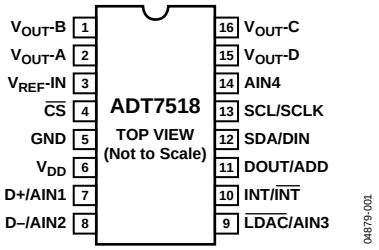

Figure 1.

GENERAL DESCRIPTION

The ADT7518[1] combines a 10-bit temperature-to-digital converter, a 10-bit 4-channel ADC, and a quad 8-bit DAC, in a 16-lead QSOP package. The part also includes a band gap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25°C.

The ADT7518 operates from a single 2.7 V to 5.5 V supply. The input voltage range on the ADC channels is 0 V to 2.25 V, and the input bandwidth is dc. The reference for the ADC channels is derived internally. The output voltage of the DAC ranges from 0 V to V_{DD}, with an output voltage settling time of 7 ms typical.

The ADT7518 provides two serial interface options: a 4-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards, and a 2-wire SMBus/I²C interface. It features a standby mode that is controlled through the serial interface.

The reference for the four DACs is derived either internally or from a reference pin. The outputs of all DACs may be updated simultaneously using the software LDAC function or the external $\overline{LDAC}$ pin. The ADT7518 incorporates a power-on reset circuit, which ensures that the DAC output powers up to 0 V and remains there until a valid write takes place.

The ADT7518's wide supply voltage range, low supply current, and SPI-/I²C-compatible interface make it ideal for a variety of applications, including personal computers, office equipment, and domestic appliances.

It is recommended that new designs use the ADT7519 rather than the ADT7518. The ADT7518's internal and external temperature accuracy spec is only valid when not using the internal reference for the on-chip DAC. The ADT7519 does not have this limitation.

[1] Protected by the following U.S. Patent Numbers: 6,169,442; 5,867,012; 5,764174. Other patents pending.

Rev. A

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REVISION HISTORY

8/04—Data Sheet Changed from Rev. 0 to Rev. A

Updated Format ..... Universal

Separate ADT7518 from
ADT7516/ADT7517/ADT7518 Data Sheet ..... Universal

Change to Equation 25

7/03—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Temperature range is as follows: A version: −40°C to +120°C. V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.25 V, unless otherwise noted.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
DAC DC PERFORMANCE[2,3]					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed monotonic over all codes.
Offset Error		±0.4	±2	% of FSR	
Gain Error		±0.3	±2	% of FSR	
Lower Deadband		20	65	mV	Lower deadband exists only if offset error is negative. See Figure 8.
Upper Deadband		60	100	mV	Upper deadband exists if $V_{REF} = V_{DD}$ and offset plus gain error is positive. See Figure 9.
Offset Error Drift[4]		−12		ppm of FSR/°C	
Gain Error Drift[4]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[4]		−60		dB	ΔV_{DD} = ±10%.
DC Crosstalk[4]		200		µV	See Figure 5.
ADC DC ACCURACY					Max V_{DD} = 5 V.
Resolution			10	Bits	
Total Unadjusted Error (TUE)		2	3	% of FSR	
Offset Error			±0.5	% of FSR	
Gain Error			±2	% of FSR	
ADC BANDWIDTH			DC	Hz	
ANALOG INPUTS[5]					
Input Voltage Range	0		2.25	V	AIN1 to AIN4. C4 = 0 in Control Configuration 3.
	0		V_{DD}	V	AIN1 to AIN4. C4 = 0 in Control Configuration 3.
DC Leakage Current			±1	µA	
Input Capacitance		5	20	pF	
Input Resistance		10		MΩ	
THERMAL CHARACTERISTICS[6] INTERNAL TEMPERATURE SENSOR					Internal reference used. Averaging on.
Accuracy @ V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C.
		±0.5	±3	°C	T_A= 0°C to +85°C.
		±2	±5	°C	T_A = −40°C to +120°C.
Accuracy @ V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C.
		±3	±5	°C	T_A = −40°C to +120°C.
Resolution			10	Bits	Equivalent to 0.25°C.
Long-Term Drift		0.25		°C	Drift over 10 years if part is operated at 55°C.
THERMAL CHARACTERISTICS[6] EXTERNAL TEMPERATURE SENSOR					External transistor = 2N3906.
Accuracy @ V_{DD} = 3.3 V ± 10%			±1.5	°C	T_A = 85°C.
			±3	°C	T_A = 0°C to +85°C.
			±5	°C	T_A = −40°C to +120°C.
Accuracy @ V_{DD} = 5 V ± 5%		±2	±3	°C	T_A = 0°C to +85°C.
		±3	±5	°C	T_A = −40°C to +120°C.
Resolution			10	Bits	Equivalent to 0.25°C.
Output Source Current		180		µA	High Level.
		11		µA	Low Level.
THERMAL CHARACTERISTICS[6]					
Thermal Voltage Output					
8-Bit DAC Output					
Resolution	1			°C	

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
Scale Factor		8.97		mV/°C	0 V to V_{REF} output. T_A = −40°C to +120°C.
		17.58		mV/°C	0 V to 2 V_{REF} output. T_A = −40°C to +120°C.
CONVERSION TIMES					Single channel mode.
Slow ADC					
V_{DD}/AIN		11.4		ms	Averaging (16 samples) on.
		712		µs	Averaging off.
Internal Temperature		11.4		ms	Averaging (16 samples) on.
		712		µs	Averaging off.
External Temperature		24.22		ms	Averaging (16 samples) on.
		1.51		ms	Averaging off.
Fast ADC					
V_{DD}/AIN		712		µs	Averaging (16 samples) on.
		44.5		µs	Averaging off.
Internal Temperature		2.14		ms	Averaging (16 samples) on.
		134		µs	Averaging off.
External Temperature		14.25		ms	Averaging (16 samples) on.
		890		µs	Averaging off.
ROUND ROBIN UPDATE RATE[5]					Time to complete one measurement cycle through all channels.
Slow ADC @ 25°C					
Averaging On		79.8		ms	AIN1 and AIN2 are selected on Pins 7 and 8.
Averaging Off		4.99		ms	AIN1 and AIN2 are selected on Pins 7 and 8.
Averaging On		94.76		ms	D+ and D− are selected on Pins 7 and 8.
Averaging Off		9.26		ms	D+ and D− are selected on Pins 7 and 8.
Fast ADC @ 25°C					
Averaging On		6.41		ms	AIN1 and AIN2 are selected on Pins 7 and 8.
Averaging Off		400.84		µs	AIN1 and AIN2 are selected on Pins 7 and 8.
Averaging On		21.77		ms	D+ and D− are selected on Pins 7 and 8.
Averaging Off		3.07		ms	D+ and D− are selected on Pins 7 and 8.
DAC EXTERNAL REFERENCE INPUT[4]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference.
V_{REF} Input Impedance		>10		MΩ	Buffered reference and power-down mode.
Reference Feedthrough		−90		dB	Frequency = 10 kHz.
Channel-to-Channel Isolation		−75		dB	Frequency = 10 kHz.
ON-CHIP REFERENCE					
Reference Voltage[4]		2.25		V	
Temperature Coefficient[4]		80		ppm/°C	
OUTPUT CHARACTERISTICS[4]					
Output Voltage [7]	0.001		V_{DD} − 0.1	V	This is a measure of the minimum and maximum drive capability of the output amplifier.
DC Output Impedance		0.5		Ω	
Short-Circuit Current		25		mA	V_{DD} = 5 V.
		16		mA	V_{DD} = 3 V.
Power-Up Time		2.5		µs	Coming out of power-down mode. V_{DD} = 5 V.
		5		µs	Coming out of power-down mode. V_{DD} = 3.3 V.
DIGITAL INPUTS[4]					
Input Current			±1	µA	V_{IN} = 0 V to V_{DD}.
V_{IL}, Input Low Voltage			0.8	V	
V_{IH}, Input High Voltage	1.89			V	
Pin Capacitance		3	10	pF	All digital inputs.
SCL, SDA Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns.
$\overline{LDAC}$ Pulse Width	20			ns	Edge triggered input.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
DIGITAL OUTPUT					
Digital High Voltage, V_{OH}	2.4			V	$I_{SOURCE} = I_{SINK} = 200$ µA.
Output Low Voltage, V_{OL}			0.4	V	$I_{OL} = 3$ mA.
Output High Current, I_{OH}			1	mA	$V_{OH} = 5$ V.
Output Capacitance, C_{OUT}			50	pF	
INT/$\overline{INT}$ Output Saturation Voltage			0.8	V	$I_{OUT} = 4$ mA.
I^2C TIMING CHARACTERISTICS [8, 9]					
Serial Clock Period, t_1	2.5			µs	Fast Mode I^2C. See Figure 2.
Data In Setup Time to SCL High, t_2	50			ns	
Data Out Stable after SCL Low, t_3	0			ns	See Figure 2.
SDA Low Setup Time to SCL Low (Start Condition), t_4	50			ns	See Figure 2.
SDA High Hold Time after SCL High (Stop Condition), t_5	50			ns	See Figure 2.
SDA and SCL Fall Time, t_6			90	ns	See Figure 2.
SPI TIMING CHARACTERISTICS[4, 10]					
$\overline{CS}$ to SCLK Setup Time, t_1	0			ns	See Figure 3.
SCLK High Pulse Width, t_2	50			ns	See Figure 3.
SCLK Low Pulse Width, t_3	50			ns	See Figure 3.
Data Access Time after SCLK Falling Edge, t_4 [11]			35	ns	
Data Setup Time Prior to SCLK Rising Edge, t_5	20			ns	See Figure 3.
Data Hold Time after SCLK Rising Edge, t_6	0			ns	See Figure 3.
$\overline{CS}$ to SCLK Hold Time, t_7	0			µs	See Figure 3.
$\overline{CS}$ to DOUT High Impedance, t_8			40	ns	See Figure 3.
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
V_{DD} Settling Time			50	ms	V_{DD} settles to within 10% of its final voltage level.
I_{DD} (Normal Mode) [12]			3	mA	$V_{DD} = 3.3$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND.
		2.2	3	mA	$V_{DD} = 5$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND.
I_{DD} (Power-Down Mode)			10	µA	$V_{DD} = 3.3$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND.
			10	µA	$V_{DD} = 5$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND.
Power Dissipation			10	mW	$V_{DD} = 3.3$ V. Normal mode.
			33	µW	$V_{DD} = 3.3$ V. Shutdown mode.

[1] See the Terminology section.
[2] DC specifications are tested with the outputs unloaded.
[3] Linearity is tested using a reduced code range: ADT7518 (Code 8 to 255).
[4] Guaranteed by design and characterization, not production tested.
[5] Round robin is the continuous sequential measurement of the following channels: V_{DD}, internal temperature, external temperature (AIN1, AIN2), AIN3, and AIN4.
[6] The temperature accuracy specifications are valid when the internal reference is not being used by the on-chip DAC. For new designs, the ADT7519 is recommended as it does not have this limitation.
[7] For the amplifier output to reach its minimum voltage, the offset error must be negative. For the amplifier output to reach its maximum voltage ($V_{REF} = V_{DD}$), the offset plus gain error must be positive.
[8] The SDA and SCL timing is measured with the input filters turned on to meet the fast-mode I^2C specification. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[9] Guaranteed by design, not production tested.
[10] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}), and timed from a voltage level of 1.6 V.
[11] Measured with the load circuit shown in Figure 4.
[12] The I_{DD} specification is valid for all DAC codes and full-scale analog input voltages. Interface inactive. All DACs and ADCs active. Load currents excluded.

DAC AC CHARACTERISTICS[1]

Table 2. V_{DD} = 2.7 V to 5.5 V, R_L = 4.7 kΩ to GND; C_L = 200 pF to GND; 4.7 kΩ to V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter[2]	Min	Typ[3]	Max	Unit	Conditions/Comments
Output Voltage Settling Time					V_{REF} = V_{DD} = 5 V
ADT7518		6	8	µs	1/4 scale to 3/4 scale change (40h to C0h)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		1		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ±0.1 V p-p
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ±0.1 V p-p. Frequency = 10 kHz.

[1] Guaranteed by design and characterization, not production tested.
[2] See the Terminology section.
[3] @ 25°C.

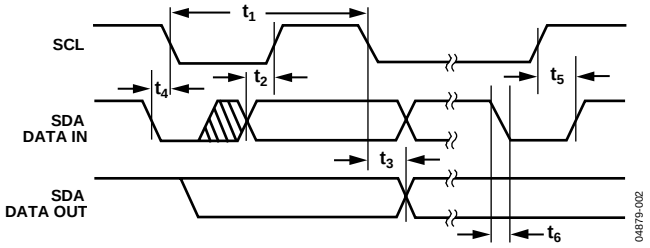


Figure 2. I²C Bus Timing Diagram

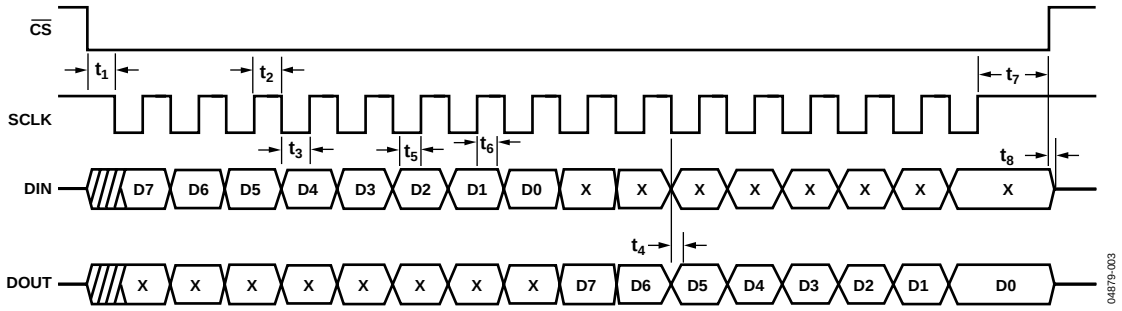


Figure 3. SPI Bus Timing Diagram

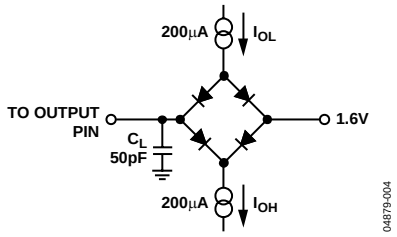


Figure 4. Load Circuit for Access Time and Bus Relinquish Time

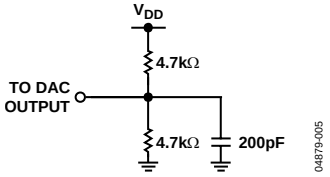


Figure 5. Load Circuit for DAC Outputs

FUNCTIONAL BLOCK DIAGRAM

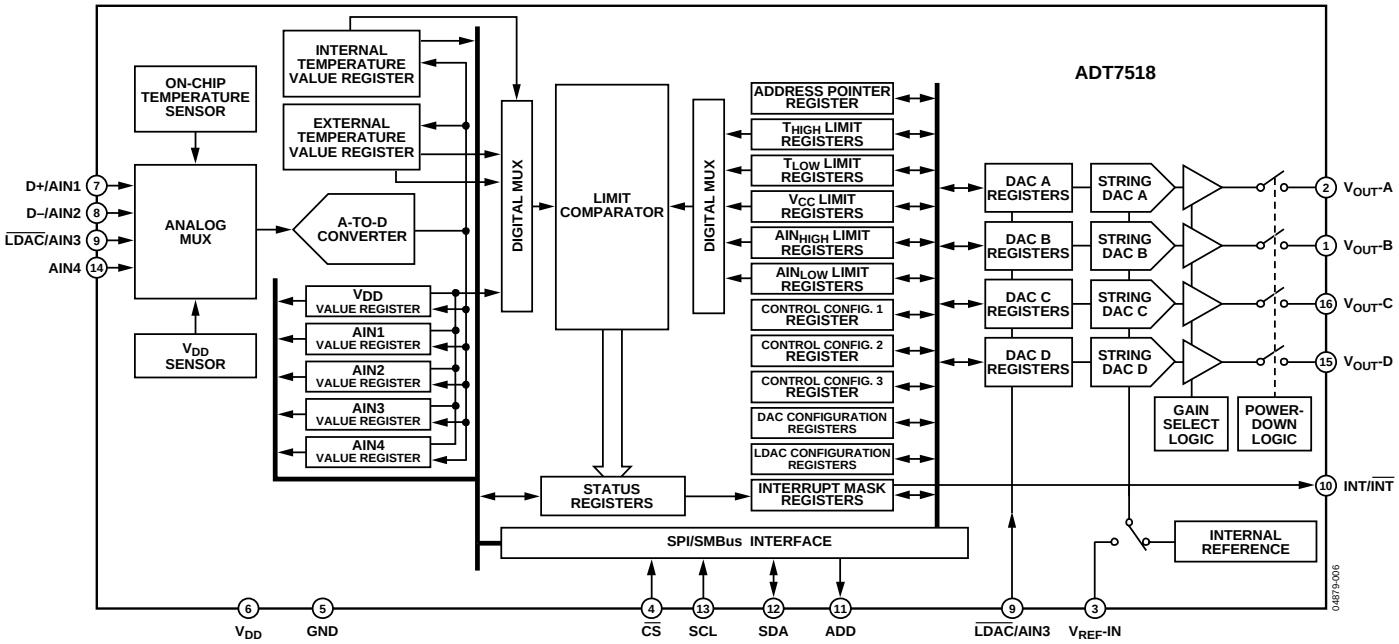


Figure 6.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +120°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
16-Lead QSOP Package	
Power Dissipation[1]	$(T_J$ max – $T_A)/\theta_{JA}$
Thermal Impedance[2]	
θ_{JA} Junction-to-Ambient	105.44°C/W
θ_{JC} Junction-to-Case	38.8°C/W
IR Reflow Soldering	
Peak Temperature	220°C (0°C/5°C)
Time at Peak Temperature	10 sec to 20 sec
Ramp-Up Rate	2°C/sec to 3°C/sec
Ramp-Down Rate	–6°C/sec

Table 4. I²C Address Selection

ADD Pin	I²C Address
Low	1001 000
Float	1001 010
High	1001 011

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Values relate to package being used on a 4-layer board.
[2] Junction-to-case resistance is applicable to components featuring a preferential flow direction, e.g., components mounted on a heat sink. Junction-to-ambient resistance is more useful for air cooled PCB-mounted components.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

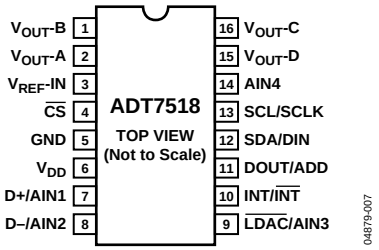


Figure 7. Pin Configuration QSOP

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}-B	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
2	V_{OUT}-A	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V_{REF}-IN	Reference Input Pin for All Four DACs. This input is buffered and has an input range from 1 V to V_{DD}.
4	$\overline{CS}$	SPI Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it enables the input register, and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pin be tied high to V_{DD} when operating the serial interface in I^2C mode.
5	GND	Ground Reference Point for All Circuitry on the Part. Analog and digital ground.
6	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground.
7	D+/AIN1	D+. Positive Connection to External Temperature Sensor. AIN1. Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
8	D–/AIN2	D–. Negative Connection to External Temperature Sensor. AIN2. Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
9	$\overline{LDAC}$/AIN3	$\overline{LDAC}$. Active Low Control Input. Transfers the contents of the input registers to their respective DAC registers. A falling edge on this pin forces any or all DAC registers to be updated if the input registers have new data. A minimum pulse width of 20 ns must be applied to the $\overline{LDAC}$ pin to ensure proper loading of a DAC register. This allows simultaneous update of all DAC outputs. Bit C3 of the Control Configuration 3 register enables the $\overline{LDAC}$ pin. Default is with the $\overline{LDAC}$ pin controlling the loading of the DAC registers. AIN3. Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
10	INT/$\overline{INT}$	Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature,V_{DD}, or AIN limits are exceeded. The default is active low. Open-drain output—needs a pull-up resistor.
11	DOUT/ADD	SPI Serial Data Output. Logic output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. Open-drain output—needs a pull-up resistor. ADD. I^2C Serial Bus Address Selection Pin. Logic input. A low on this pin gives the address 1001 000; leaving it floating gives the address 1001 010; and setting it high gives the address 1001 011. The I^2C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent changes on this pin will have no effect on the I^2C serial bus address.
12	SDA/DIN	SDA. I^2C Serial Data Input/Output. I^2C serial data to be loaded into the part's registers and read from these registers is provided on this pin. Open-drain configuration—needs a pull-up resistor. DIN. SPI Serial Data Input. Serial data to be loaded into the part's registers is provided on this pin. Data is clocked into a register on the rising edge of SCLK. Open-drain configuration—needs a pull-up resistor.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7518 and also to clock data into any register that can be written to. Open-drain configuration—needs a pull-up resistor.
14	AIN4	Analog Input. Single-ended analog input channel. Input range is 0 V to 2.25 V or 0 V to V_{DD}.
15	V_{OUT}-D	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
16	V_{OUT}-C	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.

TERMINOLOGY

Relative Accuracy

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the transfer function. Typical INL versus code plots can be seen in Figure 10, Figure 11, and Figure 12.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±0.9 LSB maximum ensures monotonicity. Typical DAC DNL versus code plots can be seen in Figure 13, Figure 14, and Figure 15.

Total Unadjusted Error (TUE)

Total unadjusted error is a comprehensive specification that includes the sum of the relative accuracy error, gain error, and offset error under a specified set of conditions.

Offset Error

This is a measure of the offset error of the DAC and the output amplifier (see Figure 8 and Figure 9). It can be negative or positive, and it is expressed in mV.

Offset Error Match

This is the difference in offset error between any two channels.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Gain Error Match

This is the difference in gain error between any two channels.

Offset Error Drift

This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Long Term Temperature Drift

This is a measure of the change in temperature error over time. It is expressed in °C. The concept of long-term stability has been used for many years to describe the amount an IC's parameter shifts during its lifetime. This is a concept that has typically been applied to both voltage references and monolithic temperature sensors. Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or so to determine this shift. Manufacturers perform accelerated lifetime testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period (typically between 500 and 1,000 hours). As a result, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

DC Power Supply Rejection Ratio (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in µV.

Reference Feedthrough

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., LDAC is high). It is expressed in dB.

Channel-to-Channel Isolation

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dB.

Major-Code Transition Glitch Energy

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011...1 to 100...00 or 100...00 to 011...11).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to. It is specified in nV-s and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s or vice versa.

Digital Crosstalk

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output, expressed in dB.

Round Robin

This term is used to describe the ADT7518 cycling through the available measurement channels in sequence, taking a measurement on each channel.

DAC Output Settling Time

This is the time required, following a prescribed data change, for the output of a DAC to reach and remain within ±0.5 LSB of the final value. A typical prescribed change is from 1/4 scale to 3/4 scale.

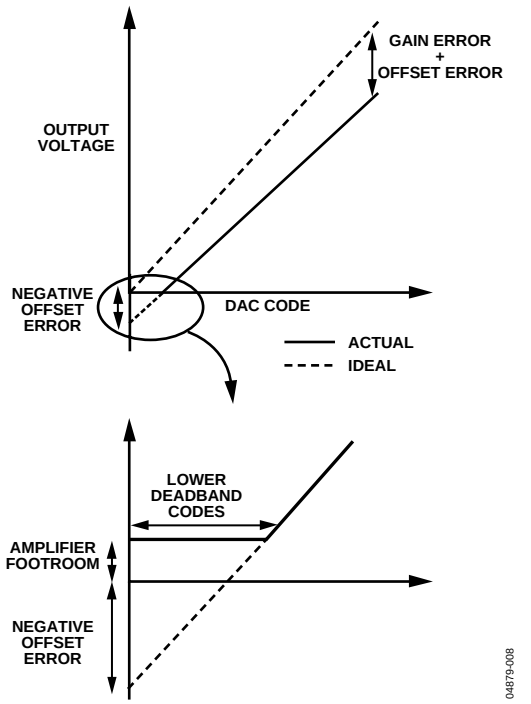


Figure 8. DAC Transfer Function with Negative Offset

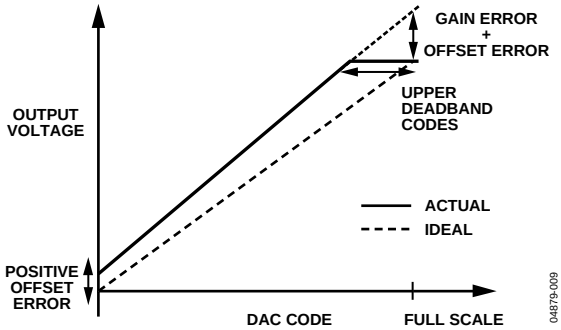


Figure 9. DAC Transfer Function with Positive Offset ($V_{REF} = V_{DD}$)

TYPICAL PERFORMANCE CHARACTERISTICS

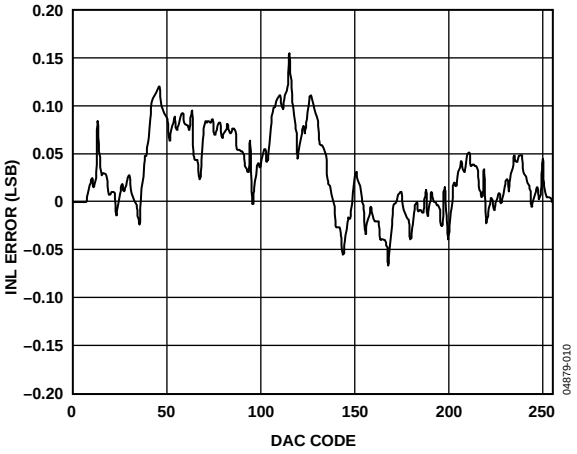


Figure 10. ADT7518 Typical DAC INL Plot

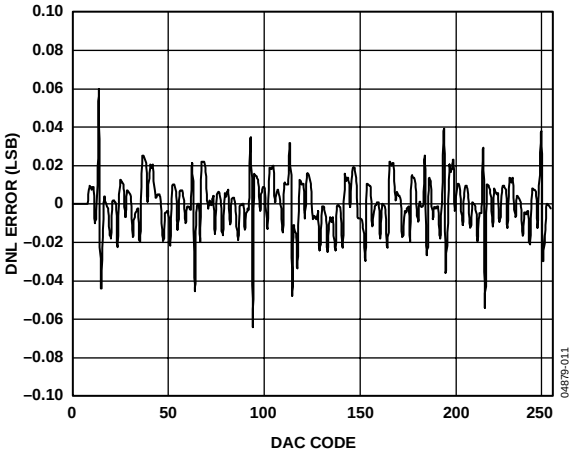


Figure 11. ADT7518 Typical DAC DNL Plot

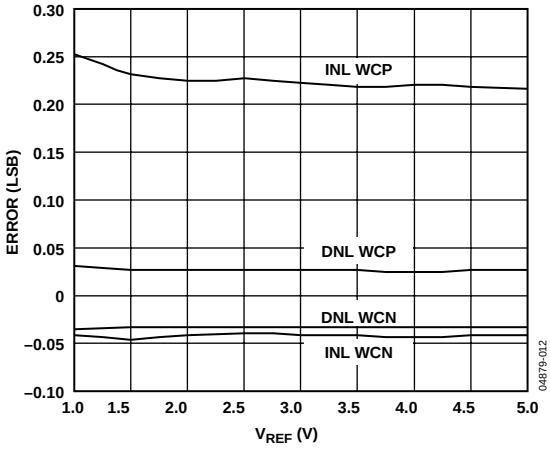


Figure 12. ADT7518 DAC INL and DNL Error vs, V_{REF}

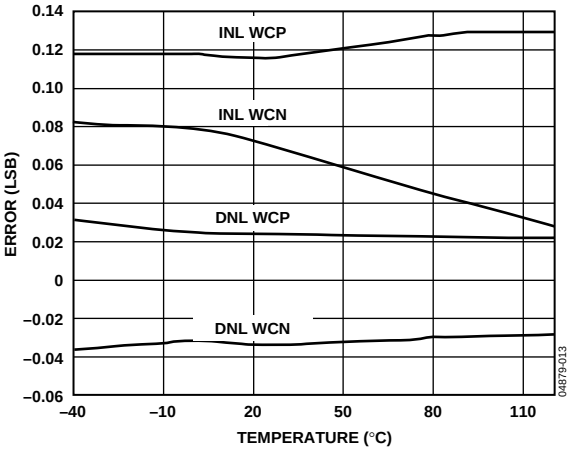


Figure 13. ADT7518 DAC INL Error and DNL Error vs. Temperature

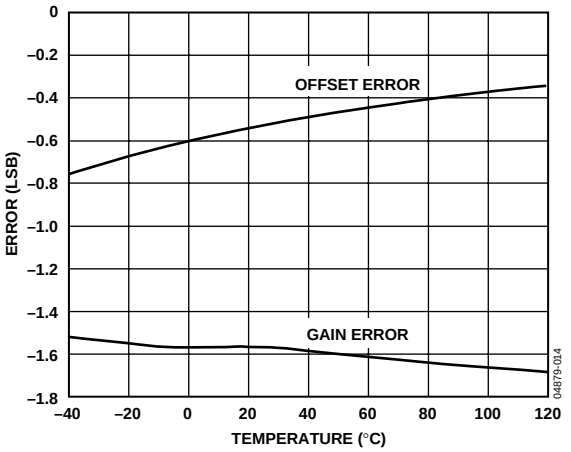


Figure 14. DAC Offset Error and Gain Error vs. Temperature

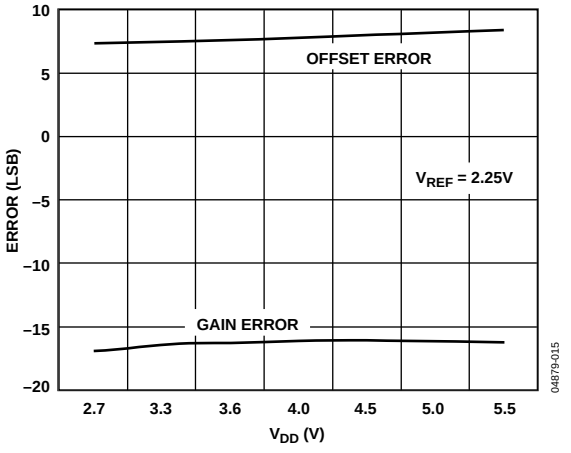


Figure 15. DAC Offset Error and Gain Error vs. V_{DD}

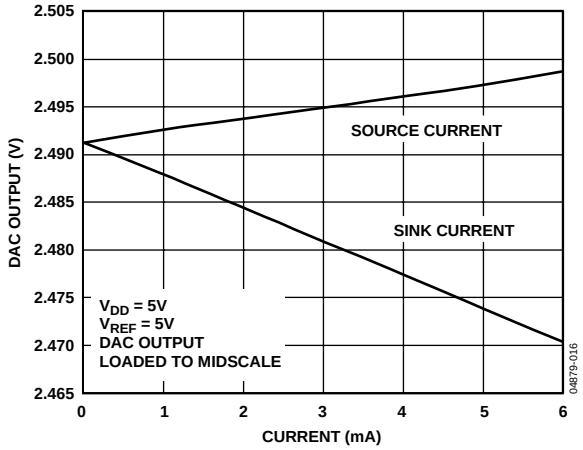


Figure 16. DAC V_{OUT} Source and Sink Current Capability

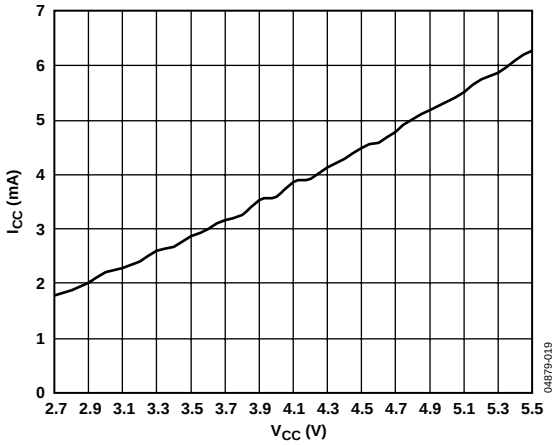


Figure 19. Power-Down Current vs. Supply Voltage @ 25°C

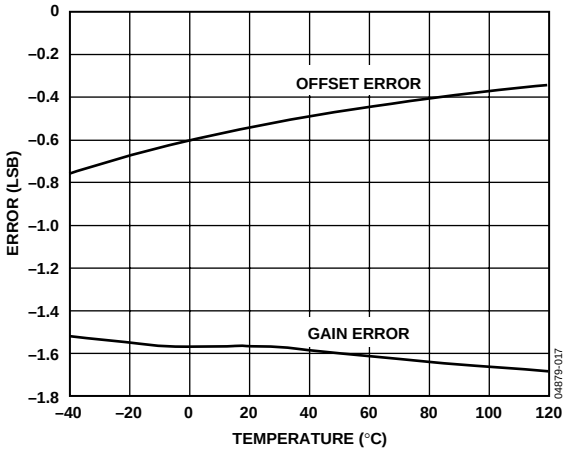


Figure 17. Supply Current vs. DAC Code

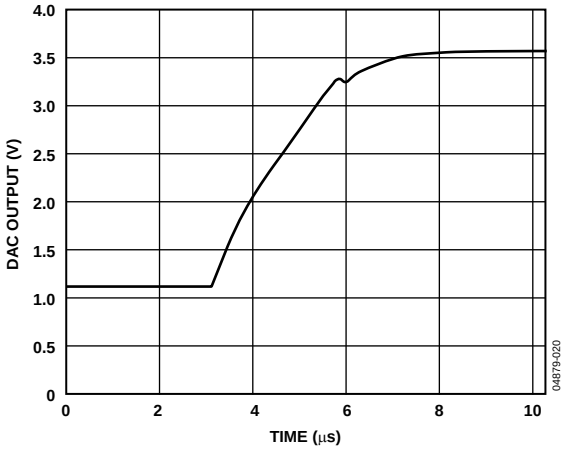


Figure 20. DAC Half-Scale Settling (1/4 to 3/4 Scale Code Change)

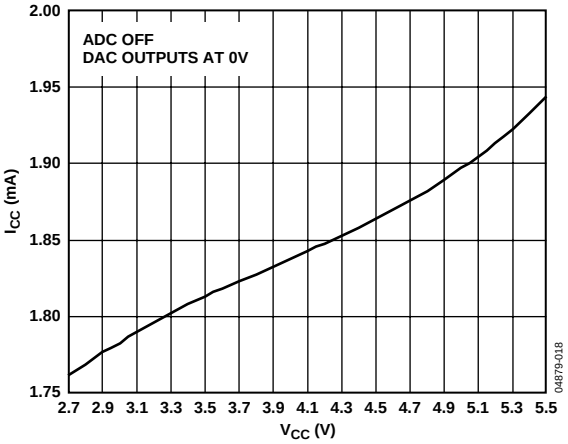


Figure 18. Supply Current vs. Supply Voltage @ 25°C

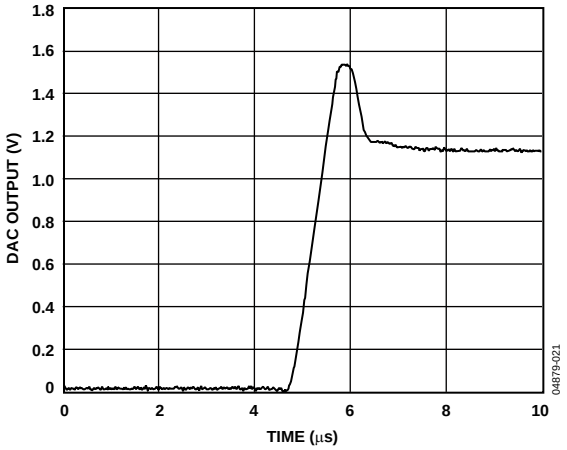


Figure 21. Exiting Power-Down to Midscale

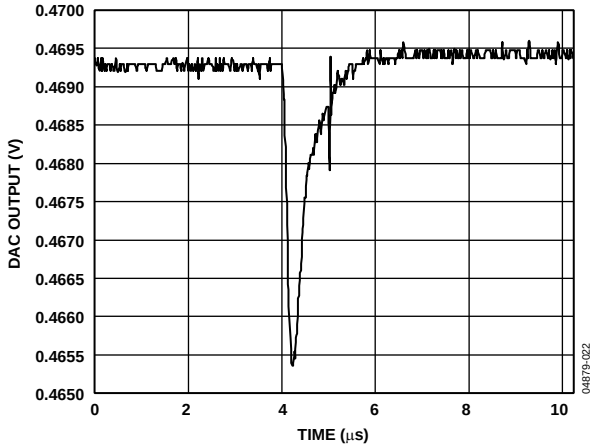


Figure 22. ADT7518 DAC Major Code Transition Glitch Energy; 0...11 to 100...00

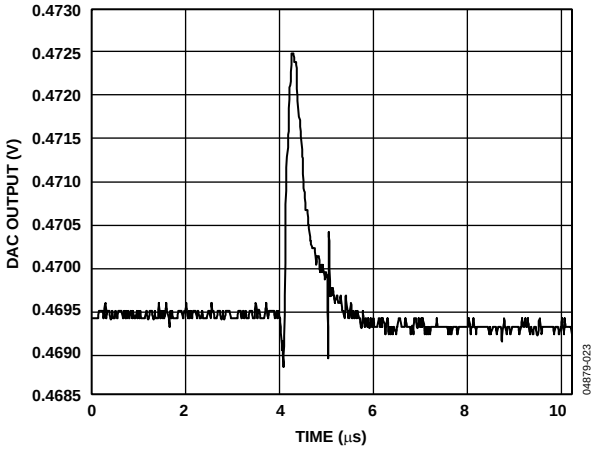


Figure 23. ADT7518 DAC Major Code Transition Glitch Energy; 100…00 to 011…11

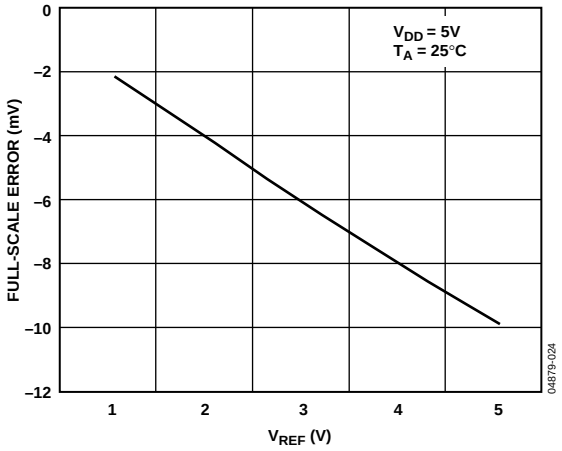


Figure 24. DAC Full-Scale Error vs. V_{REF}

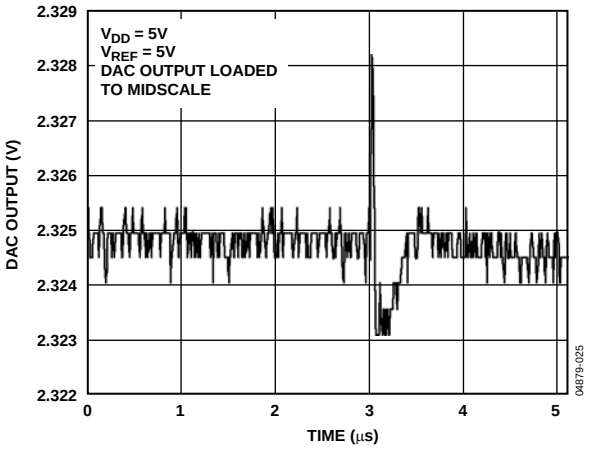


Figure 25. DAC-to-DAC Crosstalk

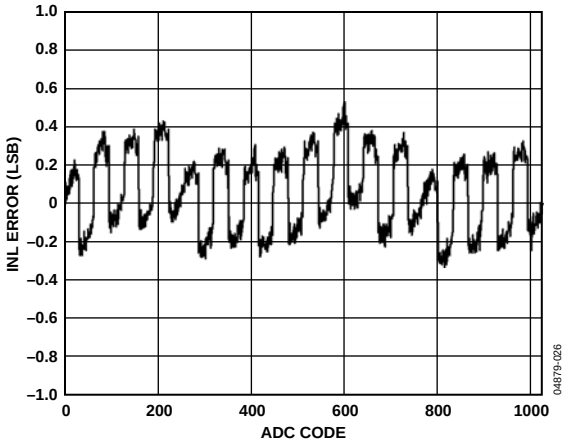


Figure 26. ADC INL with Ref = V_{DD} (3.3 V)

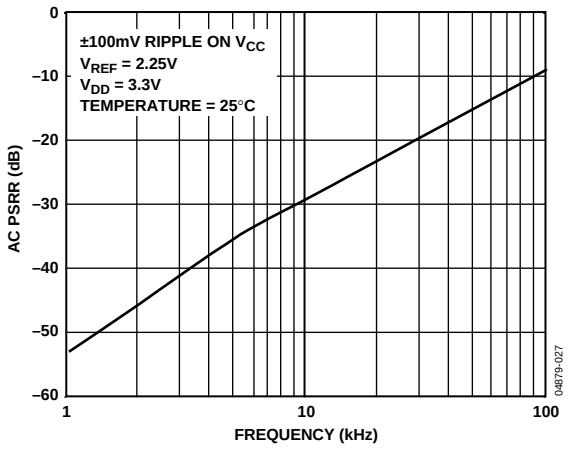


Figure 27. PSRR vs. Supply Ripple Frequency

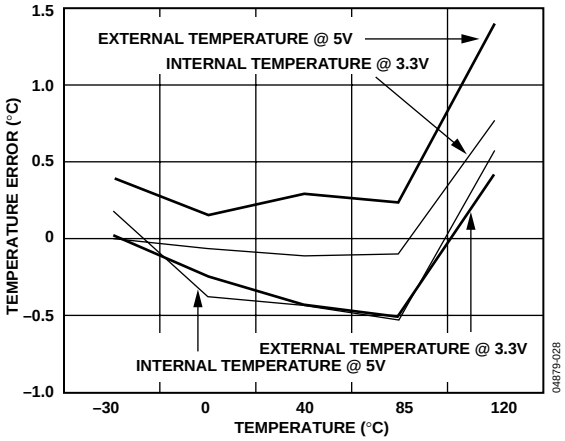


Figure 28. Internal Temperature Error @ 3.3 V and 5 V

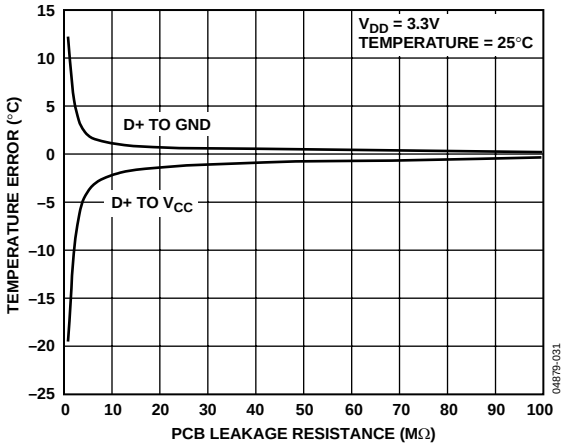


Figure 31. External Temperature Error vs. PCB Leakage Resistance

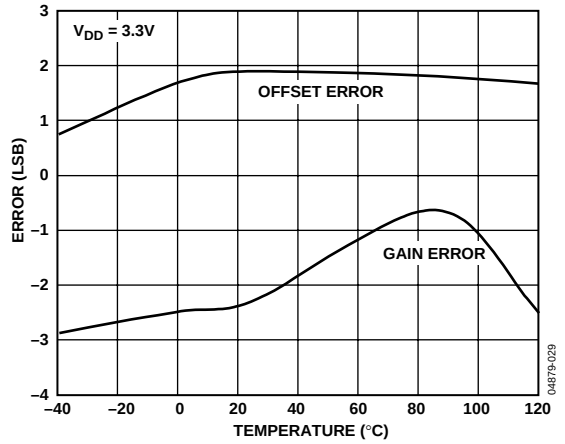


Figure 29. ADC Offset Error and Gain Error vs. Temperature

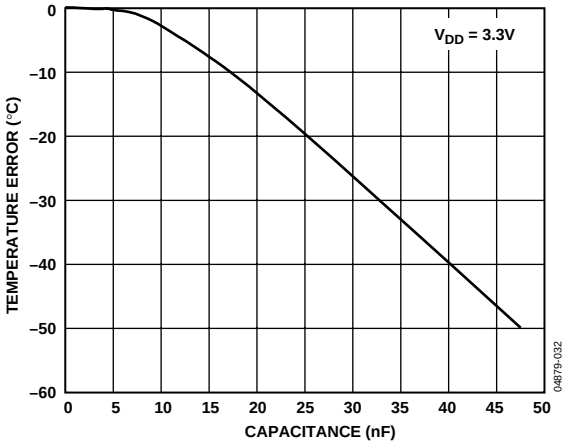


Figure 32. External Temperature Error vs. Capacitance between D+ and D–

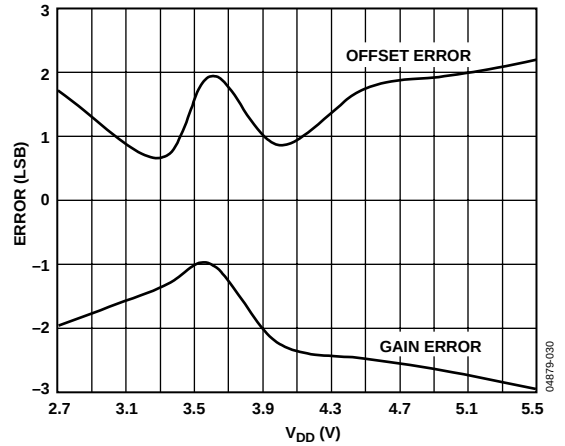


Figure 30. ADC Offset Error and Gain Error vs. V_{DD}

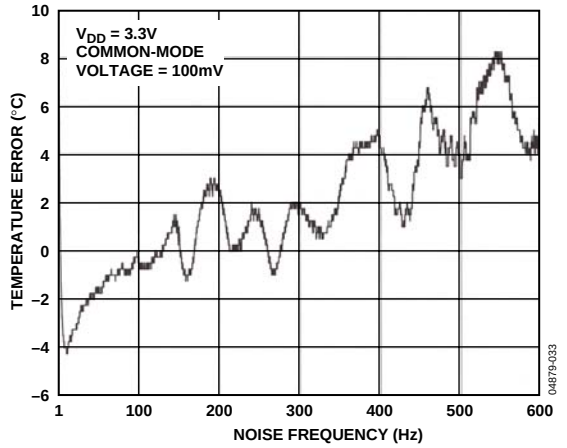


Figure 33. External Temperature Error vs. Common-Mode Noise Frequency

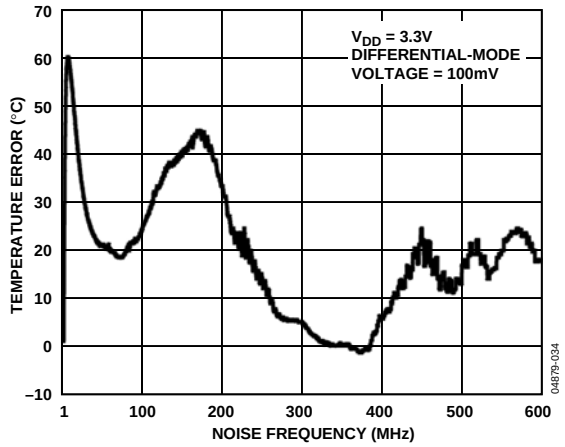


Figure 34. External Temperature Error vs. Differential-Mode Noise Frequency

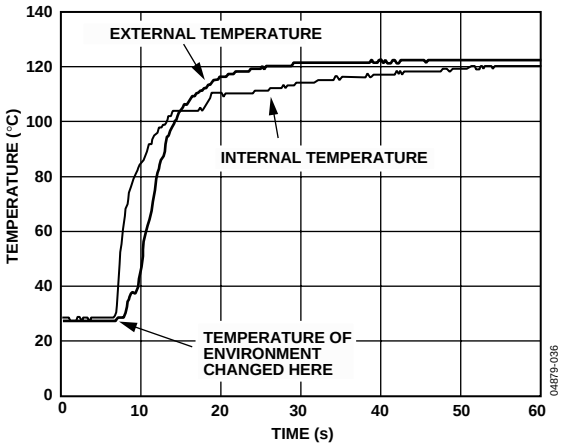


Figure 36. Temperature Sensor Response to Thermal Shock

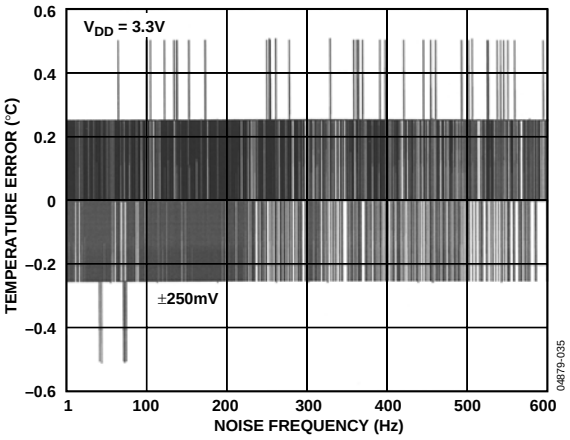


Figure 35. Internal Temperature Error vs. Power Supply Noise Frequency

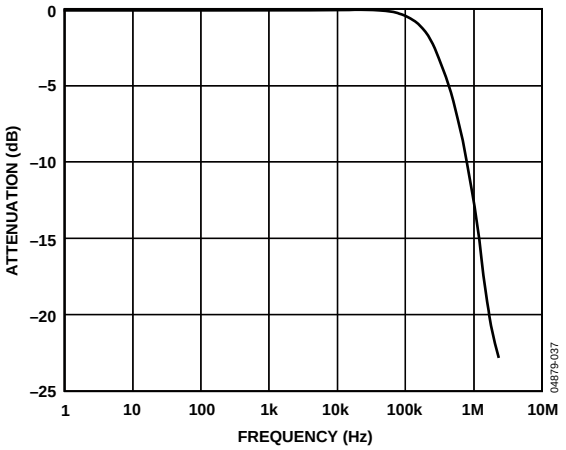


Figure 37. DAC Multiplying Bandwidth (Small Signal Frequency Response)

THEORY OF OPERATION

Directly after the power-up calibration routine, the ADT7518 goes into idle mode. In this mode, the device is not performing any measurements and is fully powered up. All four DAC outputs are at 0 V.

To begin monitoring, write to the Control Configuration 1 register (Address 18h) and set Bit C0 = 1. The ADT7518 goes into its power-up default measurement mode, which is round robin. The device then to take measurements on the V_{DD} channel, internal temperature sensor channel, external temperature sensor channel, or AIN1 and AIN2, AIN3, and finally AIN4.

Once it finishes taking measurements on the AIN4 channel, the device immediately loops back to start taking measurements on the V_{DD} channel and repeats the same cycle as before. This loop continues until the monitoring is stopped by resetting Bit C0 of the Control Configuration 1 register to 0. It is also possible to continue monitoring as well as switching to single-channel mode by writing to the Control Configuration 2 register (Address 19h) and setting Bit C4 = 1. Further explanation of the single-channel and round robin measurement modes is given in later sections.

All measurement channels have averaging enabled on them on power-up. Averaging forces the device to take an average of 16 readings before giving a final measured result. To disable averaging and consequently decrease the conversion time by a factor of 16, set Bit C5 = 1 in the Control Configuration 2 register.

There are four single-ended analog input channels on the ADT7518: AIN1 to AIN4. AIN1 and AIN2 are multiplexed with the external temperature sensor terminals D+ and D–. Bits C1 and C2 of the Control Configuration 1 register (Address 18h) are used to select between AIN1/AIN2 and the external temperature sensor. The input range on the analog input channels is dependent on whether the ADC reference used is the internal V_{REF} or V_{DD}. To meet linearity specifications, it is recommended that the maximum V_{DD} value is 5 V. Bit C4 of the Control Configuration 3 register is used to select between the internal reference or V_{DD} as the analog inputs' ADC reference.

Controlling the DAC outputs can be done by writing to the DACs' MSB and LSB registers (Addresses 10h to 17h). The power-up default setting is to have a low going pulse on the $\overline{\text{LDAC}}$ pin (Pin 9) controlling the updating of the DAC outputs from the DAC registers. Alternatively, one can configure the updating of the DAC outputs to be controlled by means other than the $\overline{\text{LDAC}}$ pin by setting Bit C3 = 1 of the Control Configuration 3 register (Address 1Ah). The DAC Configuration register (Address 1Bh) and the LDAC Configuration register (Address 1Ch) can now be used to control the DAC updating. These two registers also control the output range of the DACs and selecting between the internal or external reference. DAC A and DAC B outputs can be configured to give a voltage output proportional to the temperature of the internal and external temperature sensors, respectively.

The dual serial interface defaults to the I^2C protocol on power-up. To select and lock in the SPI protocol, follow the selection process as described in the Serial Interface Selection section. The I^2C protocol cannot be locked in, while the SPI protocol is automatically locked in on selection. The interface can be switched back to be I^2C on selection when the device is powered off and on. When using I^2C, the CS pin should be tied to either V_{DD} or GND.

There are a number of different operating modes on the ADT7518 devices and all of them can be controlled by the configuration registers. These features consist of enabling and disabling interrupts, polarity of the INT/$\overline{\text{INT}}$ pin, enabling and disabling the averaging on the measurement channels SMBus timeout and software reset.

POWER-UP CALIBRATION

It is recommended that no communication to the part be initiated until approximately 5 ms after V_{DD} has settled to within 10% of its final value. It is generally accepted that most systems take a maximum of 50 ms to power up. Power-up time is directly related to the amount of decoupling on the voltage supply line.

During the 5 ms after V_{DD} has settled, the part is performing a calibration routine. Any communication to the device during calibration will interrupt this routine, and could cause erroneous temperature measurements. If it is not possible to have V_{DD} at its nominal value by the time 50 ms has elapsed or if communication to the device has started prior to V_{DD} settling, it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken. The V_{DD} measurement is used to calibrate out any temperature measurement error due to different supply voltage values.

CONVERSION SPEED

The internal oscillator circuit used by the ADC has the capability to output two different clock frequencies. This means that the ADC is capable of running at two different speeds when doing a conversion on a measurement channel. Thus, the time taken to perform a conversion on a channel can be reduced by setting Bit C0 of the Control Configuration 3 register (Address 1Ah). This increases the ADC clock speed from 1.4 kHz to 22 kHz. At the higher clock speed, the analog filters on the D+ and D– input pins (external temperature sensor) are switched off. This is why the power-up default setting is to have the ADC working at the slow speed. The typical times for fast and slow ADC speeds are given in the specifications.

The ADT7518 powers up with averaging on. This means every channel is measured 16 times and internally averaged to reduce noise. The conversion time can also be sped up by turning off the averaging. This is done by setting Bit C5 of the Control Configuration 2 register (Address 19h) to 1.

FUNCTION DESCRIPTION—VOLTAGE OUTPUT

Digital-to-Analog Converters

The ADT7518 has four resistor string DACs fabricated on a CMOS process with resolutions of 12, 10, and 8 bits, respectively. They contain four output buffer amplifiers and are written to via I²C serial interface or SPI serial interface. See the Serial Interface section for more information.

The ADT7518 operates from a single supply of 2.7 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. All four DACs share a common reference input, V_{REF}-IN. The reference input is buffered to draw virtually no current from the reference source because it offers the source a high impedance input. The devices have a power-down mode in which all DACs may be turned off completely with a high impedance output.

Each DAC output will not be updated until it receives the LDAC command. Therefore, while the DAC registers would have been written to with a new value, this value will not be represented by a voltage output until the DACs have received the LDAC command. Reading back from any DAC register prior to issuing an LDAC command will result in the digital value that corresponds to the DAC output voltage. Thus, the digital value written to the DAC register cannot be read back until after the LDAC command has been initiated. This LDAC command can be given by either pulling the $\overline{\text{LDAC}}$ pin low (falling edge loads DACs), setting up Bits D4 and D5 of the DAC configuration register (Address 1Bh), or using the LDAC register (Address 1Ch).

When using the $\overline{\text{LDAC}}$ pin to control the DAC register loading, the low going pulse width should be 20 ns minimum. The $\overline{\text{LDAC}}$ pin has to go high and low again before the DAC registers can be reloaded.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor string DAC followed by an output buffer amplifier. The voltage at the V_{REF}-IN pin or the on-chip reference of 2.25 V provides the reference voltage for the corresponding DAC. Figure 38 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:

D = decimal equivalent of the binary code that is loaded to the DAC register:
0 to 255 for ADT7518 (8 bits)
N = DAC resolution

Resistor String

The resistor string section is shown in Figure 39. It is simply a string of resistors, each of approximately 603 Ω. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

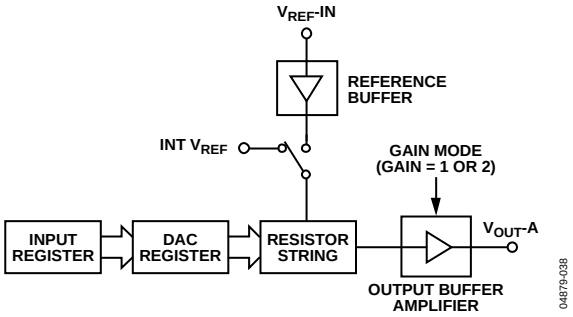


Figure 38. Single DAC Channel Architecture

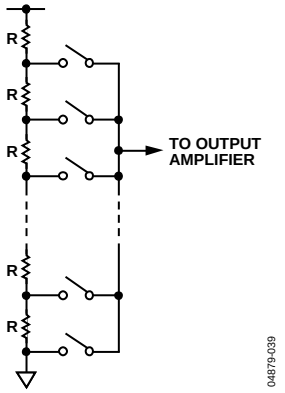


Figure 39. Resistor String

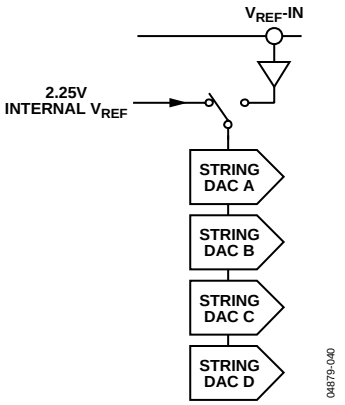


Figure 40. DAC Reference Buffer Circuit

DAC Reference Inputs

There is an input reference pin for the DACs. This reference input is buffered (see Figure 40).

The advantage with the buffered input is the high impedance it presents to the voltage source driving it. The user can have an external reference voltage as low as 1 V and as high as V_{DD}. The restriction of 1 V is due to the footroom of the reference buffer.

The $\overline{\text{LDAC}}$ configuration register controls the option to select between internal and external voltage references. The default setting is for external reference selected.

Output Amplifier

The output buffer amplifier can generate output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, gain, and offset error.

If a gain of 1 is selected (Bits 0 to 3 of the DAC configuration register = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (Bits 0 to 3 of the DAC configuration register = 1), the output range is 0.001 V to 2 V_{REF}. Because of clamping, however, the maximum output is limited to V_{DD} − 0.001 V.

The output amplifier can drive a load of 4.7 kΩ to GND or V_{DD}, in parallel with 200 pF to GND or V_{DD} (see Figure 5). The source and sink capabilities of the output amplifier can be seen in the plot of Figure 16.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 μs.

Thermal Voltage Output

The ADT7518 can output voltages that are proportional to temperature. DAC A output can be configured to represent the temperature of the internal sensor while DAC B output can be configured to represent the external temperature sensor. Bits C5 and C6 of the Control Configuration 3 register select the temperature proportional output voltage. Each time a temperature measurement is taken, the DAC output is updated. The output resolution for the ADT7518 is 8 bits with a 1°C change corresponding to 1 LSB change. The default output range is 0 V to V_{REF} and this can be increased to 0 V to 2 V_{REF}. Increasing the output voltage span to 2 V_{REF} can be done by setting D0 = 1 for DAC A (internal temperature sensor) and D1 = 1 for DAC B (external temperature sensor) in the DAC configuration register (Address 1Bh).

The output voltage is capable of tracking a maximum temperature range of −128°C to +127°C, but the default setting is −40°C to +127°C. If the output voltage range is 0 V to V_{REF}-IN (V_{REF}-IN = 2.25 V), then this corresponds to 0 V representing −40°C, and 1.48 V representing +127°C. This, of course, will give an upper deadband between 1.48 V and V_{REF}.

The internal and external analog temperature offset registers can be used to vary this upper deadband and, consequently, the temperature that 0 V corresponds to. Table 6 and Table 7 give examples of how this is done using a DAC output voltage span of V_{REF} and 2 V_{REF}, respectively. Simply write in the temperature value, in twos complement format, at which 0 V is to start. For example, if using the DAC A output and 0 V to start at −40°C, program D8h into the internal analog temperature offset register (Address 21h). This is an 8-bit register and has a temperature offset resolution of only 1°C for all device models. Use the formulas following the tables to determine the value to program into the offset registers.

Table 6. Thermal Voltage Output (0 V to V_{REF})

O/P Voltage (V)	Default °C	Max °C	Sample °C
0	−40	−128	0
0.5	+17	−71	+56
1	+73	−15	+113
1.12	+87	−1	+127
1.47	+127	+39	UDB*
1.5	UDB*	+42	UDB*
2	UDB*	+99	UDB*
2.25	UDB*	+127	UDB*

* Upper deadband has been reached. DAC output is not capable of increasing. See Figure 9.

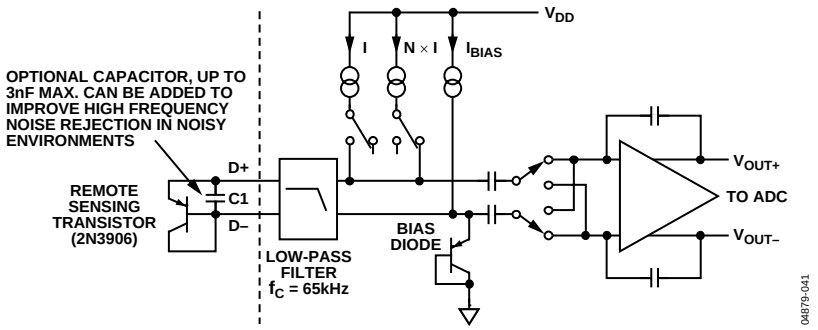


Figure 41. Signal Conditioning for External Diode Temperature Sensor

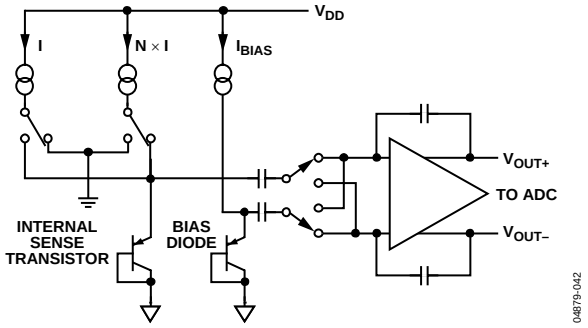


Figure 42. Top Level Structure of Internal Temperature Sensor

Table 7. Thermal Voltage Output (0 V to 2 V_{REF})

O/P Voltage (V)	Default °C	Max °C	Sample °C
0	–40	–128	0
0.25	–26	–114	+14
0.5	+12	–100	+28
0.75	+3	–85	+43
1	+17	–71	+57
1.12	+23	–65	+63
1.47	+43	–45	+83
1.5	+45	–43	+85
2	+73	–15	+113
2.25	+88	0	+127
2.5	+102	+14	UDB*
2.75	+116	+28	UDB*
3	UDB*	+42	UDB*
3.25	UDB*	+56	UDB*
3.5	UDB*	+70	UDB*
3.75	UDB*	+85	UDB*
4	UDB*	+99	UDB*
4.25	UDB*	+113	UDB*
4.5	UDB*	+127	UDB*

* Upper deadband has been reached. DAC output is not capable of increasing. See Figure 9.

Negative temperatures:

$$Offset\ Register\ Code(d) = (0\ V\ Temp) + 128$$

where:
D7 of Offset Register Code is set to 1 for negative temperatures.

Example:

$$Offset\ Register\ Code(\mathrm{d}) = (-40) + 128 = 88\mathrm{d} = 58\mathrm{h}$$

Since a negative temperature has been inserted into the equation, DB7 (MSB) of the offset register code is set to 1. Therefore 58h becomes D8h.

58h + DB7(1) = D8h

Positive temperatures:

$$Offset\ Register\ Code\ (\mathrm{d}) = 0\ V\ Temp$$

Example:

Offset Register Code (d) = 10d = 0Ah

The following equation is used to work out the various temperatures for the corresponding 8-bit DAC output:

$$8\text{-}Bit\ Temp = (DAC\ O/P \div 1\ LSB) + (0\ V\ Temp)$$

For example, if the output is 1.5 V, V_{REF}-IN = 2.25 V, 8-bit DAC has an LSB size = 2.25 V/256 = 8.79 x 10^{-3}, and 0 V temperature is at –128°C, then the resultant temperature is

$$(1.5 \div 8.79 \times 10^{-3}) + (-128) = +43°C$$

Figure 43 shows a graph of the DAC output versus temperature for a V_{REF}-IN = 2.25 V.

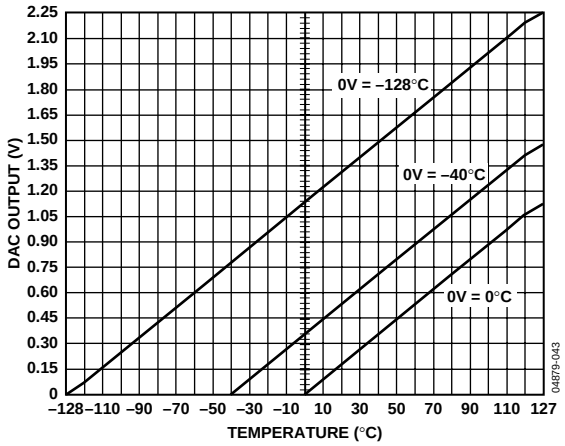


Figure 43. DAC Output vs. Temperature V_{REF}-IN = 2.25 V

FUNCTIONAL DESCRIPTION—ANALOG INPUTS

Single-Ended Inputs

The ADT7518 offers four single-ended analog input channels. The analog input range is from 0 V to 2.25 V, or 0 V to V_{DD}. To maintain the linearity specification, it is recommended that the maximum V_{DD} value be set at 5 V. Selection between the two input ranges is done by Bit C4 of the Control Configuration 3 register (Address 1Ah). Setting this bit to 0 sets up the analog input ADC reference to be sourced from the internal voltage reference of 2.25 V. Setting the bit to 1 sets up the ADC reference to be sourced from V_{DD}.

The ADC resolution is 10 bits and is mostly suitable for dc input signals. Bits C1:2 of the Control Configuration 1 register (Address 18h) are used to set up Pins 7 and 8 as AIN1 and AIN2. Figure 44 shows the overall view of the 4-channel analog input path.

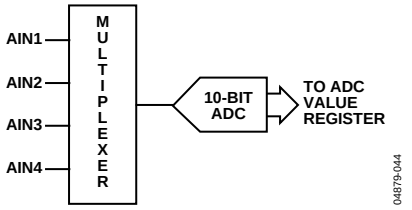


Figure 44. Quad Analog Input Path

Converter Operation

The analog input channels use a successive approximation ADC based on a capacitor DAC. Figure 45 and Figure 46 show simplified schematics of the ADC. Figure 45 shows the ADC during acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.

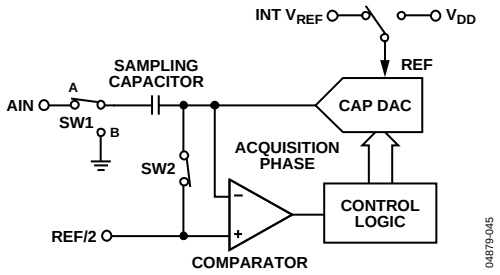


Figure 45. ADC Acquisition Phase

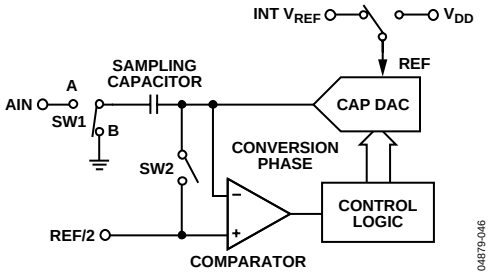


Figure 46. ADC Conversion Phase

When the ADC eventually goes into conversion phase (see Figure 46), SW2 opens and SW1 moves to position B, causing the comparator to become unbalanced. The control logic and the DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 47 shows the ADC transfer function for the analog inputs.

ADC TRANSFER FUNCTION

The output coding of the ADT7518 analog inputs is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB). The LSB is $V_{DD}/1024$ or internal $V_{REF}/1024$, internal V_{REF} = 2.25 V. The ideal transfer characteristic is shown in Figure 47.

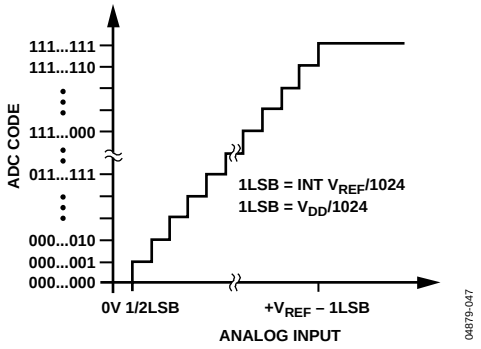


Figure 47. Single-Ended Transfer Function

To work out the voltage on any analog input channel, the following method can be used:

1 LSB = *reference* (v)/1024

Convert the value read back from the AIN value register into a decimal format.

$$AIN\ voltage = AIN\ value(d) \times LSB\ size$$

d = decimal

Example:

Internal reference used. Therefore V_{REF} = 2.25 V.

$AIN\ value$ = 512d

$$1\ LSB\ size = 2.25\ V / 1024 = 2.197 \times 10^{-3}$$

$$AIN\ voltage = 512 \times 2.197 \times 10^{-3} = 1.125\ V$$

Analog Input ESD Protection

Figure 48 shows the input structure on any of the analog input pins that provides ESD protection. The diode provides the main ESD protection for the analog inputs. Care must be taken that the analog input signal never drops below the GND rail by more than 200 mV. If this happens, the diode will become forward-biased and start conducting current into the substrate. The 4 pF capacitor is the typical pin capacitance and the resistor is a lumped component made up of the on-resistance of the multiplexer switch.

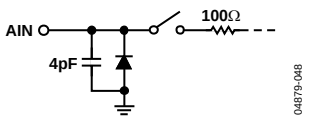


Figure 48. Equivalent Analog Input ESD Circuit

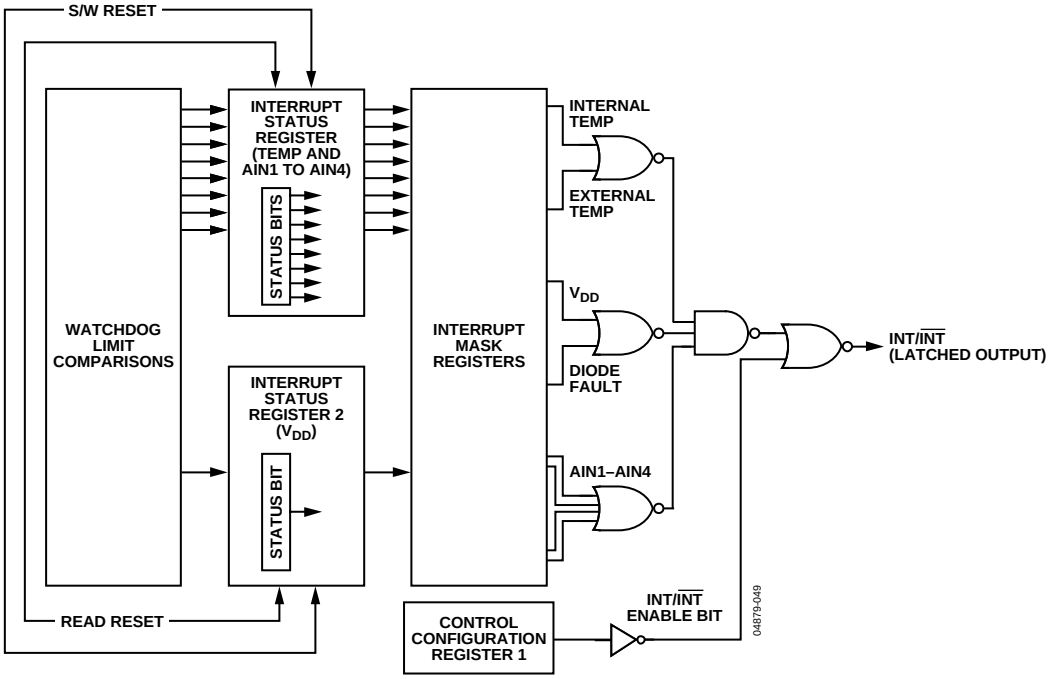


Figure 49. Interrupt Structure

AIN Interrupts

The measured results from the AIN inputs are compared with the AIN V_{HIGH} (greater than comparison) and V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the AIN inputs exceed or equal the limit registers. These voltage limits are stored in on-chip registers. Note that the limit registers are 8 bits long while the AIN conversion result is 10 bits long. If the voltage limits are not masked out, then any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address = 00h) and one or more out-of-limit results will cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application. Figure 49 shows the interrupt structure for the ADT7518. It gives a block diagram representation of how the various measurement channels affect the INT/$\overline{INT}$ pin.

FUNCTIONAL DESCRIPTION—MEASUREMENT

Temperature Sensor

The ADT7518 contains an ADC with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7518 is operating in single-channel mode, the ADC continually processes the measurement taken on one channel only. This channel is preselected by Bits C0:C2 in the Control Configuration 2 register (Address 19h). When in round robin mode, the analog input multiplexer sequentially selects the V_{DD} input channel, the on-chip temperature sensor to measure its internal temperature, either the external temperature sensor or AIN1 and AIN2, AIN3, and then AIN4. These signals are digitized by the ADC and the results are stored in the various value registers.

The measured results from the temperature sensors are compared with the internal and external T_{HIGH}, T_{LOW} limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register. One or more out-of-limit results will cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting.

Theoretically, the temperature measuring circuit can measure temperatures from −128°C to +127°C with a resolution of 0.25°C. However, temperatures outside T_A are outside the guaranteed operating temperature range of the device. Temperature measurement from −128°C to +127°C is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single-channel measurement mode. The temperature is measured 16 times and internally averaged to reduce noise. In single-channel mode, the part is continuously monitoring the selected channel, i.e., as soon as one measurement is taken another one is started on the same channel. The total time to measure a temperature channel with the ADC operating at slow speed is typically 11.4 ms (712 µs × 16) for the internal temperature sensor and 24.22 ms (1.51 ms × 16) for the external temperature sensor. The new temperature value is stored in two 8-bit registers and is ready for reading by the I²C or SPI interface. The user has the option of disabling the averaging by setting Bit 5 in the Control Configuration 2 register (Address 19h). The ADT7518 defaults on power-up with averaging enabled.

The second method is applicable when the part is in round robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode, the part continuously measures all channels.

Temperature measurement is also initiated after every read or write to the part when the part is in either single-channel measurement mode or round robin measurement mode.

Once serial communication has started, any conversion in progress is stopped and the ADC is reset. Conversion starts again immediately after the serial communication has finished. The temperature measurement proceeds normally as described in the preceding section.

V_{DD} Monitoring

The ADT7518 also has the ability to monitor its own power supply. The part measures the voltage on its V_{DD} pin to a resolution of 10 bits. The resulting value is stored in two 8-bit registers; the two LSBs are stored in register address 03h and the eight MSBs are stored in Register Address 06h. This allows the option of doing just a 1-byte read if 10-bit resolution is not important. The measured result is compared with the V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked, any out-of-limit comparison generates a flag in the Interrupt Status 2 register and one or more out-of-limit results will cause the INT/$\overline{\text{INT}}$ output to pull either high or low, depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel along with the internal, external, and AIN channels. The user can select the V_{DD} channel for single-channel measurement by setting Bit C4 = 1 and setting Bits C0:C2 to all 0s in the Control Configuration 2 register.

When measuring the V_{DD} value, the reference for the ADC is sourced from the internal reference. Table 8 shows the data format. As the maximum V_{DD} voltage measurable is 7 V, internal scaling is performed on the V_{DD} voltage to match the 2.25 V internal reference value. Below is an example of how the transfer function works.

V_{DD} = 5 V
ADC Reference = 2.25 V
1 *LSB* = *ADC Reference*/2^{10}
= 2.25/1024
= 2.226 mV
Scale Factor = *Full-Scale* V_{CC}/*ADC Reference*
= 7/2.25
= 3.07
Conversion Result = V_{DD}/(*Scale Factor* × *LSB size*)
= 5/(3.07 × 2.226 mV)
= 2 DCh

Table 8. V_{DD} Data Format (V_{REF} = 2.25 V)

	Digital Output	
V_{DD} Value (V)	Binary	Hex
2.7	01 1000 1011	18B
3	01 1011 0111	1B7
3.5	10 0000 0000	200
4	10 0100 1001	249
4.5	10 1001 0010	292
5	10 1101 1100	2DC
5.5	11 0010 0101	325
6	11 0110 1110	36E
6.5	11 1011 0111	3B7
7	11 1111 1111	3FF

On-Chip Reference

The ADT7518 has an on-chip 1.2 V band gap reference, which is gained up by a switched capacitor amplifier to give an output of 2.25 V. The amplifier is powered up for the duration of the device monitoring phase and is powered down once monitoring is disabled. This saves on current consumption. The internal reference is used as the reference for the ADC. The ADC is used for measuring V_{DD}, internal temperature sensor, external temperature sensor, and AIN inputs. The internal reference is always used when measuring V_{DD}, and the internal and external temperature sensors. The external reference is the default power-up reference for the DACs.

Round Robin Measurement

On power-up, the ADT7518 goes into round robin mode but monitoring is disabled. Setting Bit C0 of the Configuration Register 1 to 1 enables conversions. It sequences through all the available channels, taking a measurement from each in the following order: V_{DD}, internal temperature sensor, external temperature sensor/(AIN1 and AIN2), AIN3, and AIN4. Pin 7 and Pin 8 can be configured to be either external temperature sensor pins or standalone analog input pins. Once conversion is completed on the AIN4 channel, the device loops around for another measurement cycle. This method of taking a measurement on all the channels in one cycle is called round robin. Setting Bit C4 of Control Configuration 2 (Address 19h) disables the round robin mode and in turn sets up the single-channel mode. The single-channel mode is where only one channel, e.g., the internal temperature sensor, is measured in each conversion cycle.

The time taken to monitor all channels will normally not be of interest, since the most recently measured value can be read at any time. For applications where the round robin time is important, typical times at 25°C are given in the specifications.

Single-Channel Measurement

Setting C4 of the Control Configuration 2 register enables the single-channel mode and allows the ADT7518 to focus on one channel only. A channel is selected by writing to Bits C0:C2 in the Control Configuration 2 register. For example, to select the V_{DD} channel for monitoring, write to the Control Configuration

2 register and set C4 to 1 (if not done so already), then write all 0s to Bits C0:C2. All subsequent conversions will be done on the V_{DD} channel only. To change the channel selection to the internal temperature channel, write to the Control Configuration 2 register and set C0 = 1. When measuring in single-channel mode, conversions on the channel selected occur directly after each other. Any communication to the ADT7518 stops the conversions, but they are restarted once the read or write operation is completed.

Internal Temperature Measurement

The ADT7518 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the Internal Temperature Value register. Because both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 9. The thermal characteristics of the measurement sensor could change and, therefore, an offset is added to the measured value to enable the transfer function to match the thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the internal temperature offset register.

External Temperature Measurement

The ADT7518 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, because the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out, the technique is unsuitable for mass production.

The technique used in the ADT7518 is to measure the change in V_{BE} when the device is operated at two different currents. This is given by

$$\Delta V_{BE} = KT / q \times 1n(N)$$

where:

K is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in kelvins.
N is the ratio of the two currents.

Figure 41 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. A 2N3906 is recommended as the external transistor.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the Layout Considerations section for more information on C1.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a low-pass filter to remove noise, then to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

Layout Considerations

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADT7518 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided, this distance can be 4 inches to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks, if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended.

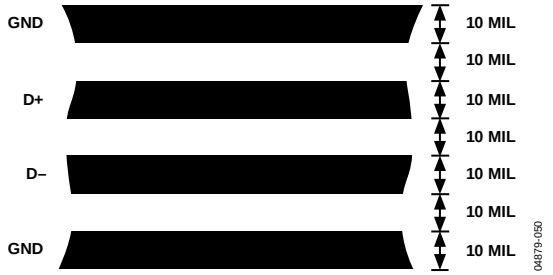


Figure 50. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature. Thermocouple effects should not be a major problem because 1°C corresponds to about 240 µV, and thermocouple voltages are about 3 µV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.

5. Place 0.1 µF bypass and 2,200 pF input filter capacitors close to the ADT7518.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted-pair cable is recommended. This will work up to about 6 feet to 12 feet.
7. For long distances (up to 100 feet), use shielded twisted-pair cable, such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADT7518. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. Series resistance of 1 Ω introduces about 0.5°C error.

Temperature Value Format

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255°C. The internal temperature sensor is guaranteed to a low value limit of –40°C. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Table 9.

The result of the internal or external temperature measurements is stored in the temperature value registers, and is compared with limits programmed into the internal or external high and low registers.

Table 9. Temperature Data Format (Internal and External Temperature)

Temperature	Digital Output
–40°C	11 0110 0000
–25°C	11 1001 1100
–10°C	11 1101 1000
–0.25°C	11 1111 1111
0°C	00 0000 0000
+0.25°C	00 0000 0001
+10°C	00 0010 1000
+25°C	00 0110 0100
+50°C	00 1100 1000
+75°C	01 0010 1100
+100°C	01 1001 0000
+105°C	01 1010 0100
+125°C	01 1111 0100

Temperature Conversion Formula:

Positive Temperature = ADC Code/4
Negative Temperature = (ADC Code – 512)/4*
*where DB9 is removed from the ADC code.

Interrupts

The measured results from the internal temperature sensor, external temperature sensor, V_{DD} pin, and AIN inputs are compared with the T_{HIGH}/V_{HIGH} (greater than comparison) and T_{LOW}/V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the measurement exceeds or equals the limit registers. These limits are stored in on-chip registers. Note that the limit registers are 8 bits long while the conversion results are 10 bits long. If the limits are not masked, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register (Address 00h) and Interrupt Status 2 register (Address 01h). One or more out-of-limit results will cause the INT/$\overline{\text{INT}}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application.

Figure 49 shows the interrupt structure for the ADT7518. It gives a block diagram representation of how the various measurement channels affect the INT/$\overline{\text{INT}}$ pin.

ADT7518 REGISTERS

The ADT7518 contains registers that are used to store the results of external and internal temperature measurements, V_{DD} value measurements, analog input measurements, high and low temperature limits, supply voltage and analog input limits, to set output DAC voltage levels, to configure multipurpose pins, and generally to control the device. A description of these registers follows.

The register map is divided into registers of 8 bits. Each register has its own individual address, but some consist of data that is linked to other registers. These registers hold the 10-bit conversion results of measurements taken on the temperature, V_{DD}, and AIN channels. For example, the eight MSBs of the V_{DD} measurement are stored in Register Address 06h, while the two LSBs are stored in Register Address 03h. These types of registers are linked such that when the LSB register is read first, the MSB registers associated with that LSB register are locked to prevent any updates. To unlock these MSB registers, the user has only to read any one of them, which will have the effect of unlocking all previously locked MSB registers. So, for the preceding example, if Register 03h was read first, MSB Registers 06h and 07h would be locked to prevent any updates to them. If Register 06h were read, this register and Register 07h would be subsequently unlocked.

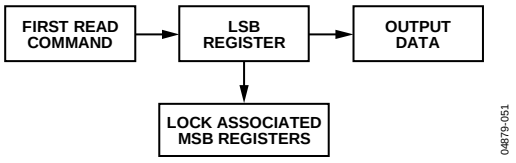


Figure 51. Phase 1 of 10-Bit Read

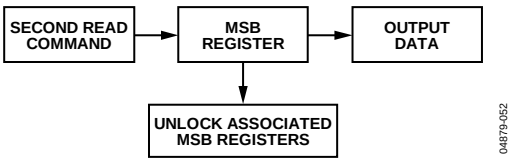


Figure 52. Phase 2 of 10-Bit Read

If an MSB register is read first, its corresponding LSB register is not locked, leaving the user with the option of just reading back 8 bits (MSB) of a 10-bit conversion result. Reading an MSB register first does not lock other MSB registers, and likewise reading an LSB register first does not lock other LSB registers.

Table 10. ADT7518 Registers

RD/WR Address	Name	Power-On Default
00h	Interrupt Status 1	00h
01h	Interrupt Status 2	00h
02h	Reserved	
03h	Internal Temp and V_{DD} LSBs	00h
04h	External Temp and AIN1 to AIN4 LSBs	00h
05h	Reserved	00h
06h	V_{DD} MSBs	xxh
07h	Internal Temp MSBs	00h
08h	External Temp MSBs/AIN1 MSBs	00h
09h	AIN2 MSBs	00h
0Ah	AIN3 MSBs	00h
0Bh	AIN4 MSBs	00h
0Ch–10h	Reserved	00h
11h	DAC A MSBs	00h
12h	Reserved	00h
13h	DAC B MSBs	00h
14h	Reserved	00h
15h	DAC C MSBs	00h
16h	Reserved	00h
17h	DAC D MSBs	00h
18h	Control Configuration 1	00h
19h	Control Configuration 2	00h
1Ah	Control Configuration 3	00h
1Bh	DAC Configuration	00h
1Ch	LDAC Configuration	00h
1Dh	Interrupt Mask 1	00h
1Eh	Interrupt Mask 2	00h
1Fh	Internal Temp Offset	00h
20h	External Temp Offset	00h
21h	Internal Analog Temp Offset	D8h
22h	External Analog Temp Offset	D8h
23h	V_{DD} V_{HIGH} Limit	C7h
24h	V_{DD} V_{LOW} Limit	62h
25h	Internal T_{HIGH} Limit	64h
26h	Internal T_{LOW} Limit	C9h
27h	External T_{HIGH}/AIN1 V_{HIGH} Limits	FFh
28h	External T_{LOW}/AIN1 V_{LOW} Limits	00h
29h–2Ah	Reserved	
2Bh	AIN2 V_{HIGH} Limit	FFh
2Bh	AIN2 V_{HIGH} Limit	FFh
2Ch	AIN2 V_{LOW} Limit	00h
2Dh	AIN3 V_{HIGH} Limit	FFh
2Eh	AIN3 V_{LOW} Limit	00h
2Fh	AIN4 V_{HIGH} Limit	FFh
30h	AIN4 V_{LOW} Limit	00h
31h–4Ch	Reserved	
4Dh	Device ID	03h/0Bh/07h
4Eh	Manufacturer's ID	41h
4Fh	Silicon Revision	04h
50h–7Eh	Reserved	00h
7Fh	SPI Lock Status	00h
80h–FFh	Reserved	00h

Interrupt Status 1 Register (Read-Only) [Address = 00h]

This 8-bit read-only register reflects the status of some of the interrupts that can cause the INT/$\overline{\text{INT}}$ pin to go active. This register is reset by a read operation, provided that any out-of-limit event has been corrected. It is also reset by a software reset.

Table 11. Interrupt Status 1 Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

Table 12.

Bit	Function
D0	1 when the internal temperature value exceeds T_{HIGH} limit. Any internal temperature reading greater than the set limit will cause an out-of-limit event.
D1	1 when internal temperature value exceeds T_{LOW} limit. Any internal temperature reading less than or equal to the set limit will cause an out-of-limit event.
D2	This status bit is linked to the configuration of Pins 7 and 8. If configured for the external temperature sensor, this bit is 1 when the external temperature value the exceeds T_{HIGH} limit. The default value for this limit register is –1°C, so any external temperature reading greater than the set limit will cause an out-of-limit event. If configured for AIN1 and AIN2, this bit is 1 when AIN1 input voltage exceeds V_{HIGH} or V_{LOW} limits.
D3	1 when external temperature value exceeds T_{LOW} limit. The default value for this limit register is 0°C, so any external temperature reading less than or equal to the set limit will cause an out-of-limit event.
D4	1 Indicates a fault (open or short) for the external temperature sensor.
D5	1 when AIN2 voltage is greater than its corresponding V_{HIGH} limit. 1 when AIN2 voltage is less than or equal to its corresponding V_{LOW} limit.
D6	1 when AIN3 voltage is greater than its corresponding V_{HIGH} limit. 1 when AIN3 voltage is less than or equal to its corresponding V_{LOW} limit.
D7	1 when AIN4 voltage is greater than its corresponding V_{HIGH} limit. 1 when AIN4 voltage is less than or equal to its corresponding V_{LOW} limit.

Interrupt Status 2 Register (Read-Only) [Address = 01h]

This 8-bit read-only register reflects the status of the V_{DD} interrupt that can cause the INT/$\overline{\text{INT}}$ pin to go active. This register is reset by a read operation, provided that any out-of-limit event has been corrected. It is also reset by a software reset.

Table 13. Interrupt Status 2 Register

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	0*	N/A	N/A	N/A	N/A

*Default settings at power-up.

Table 14.

Bit	Function
D4	1 when V_{DD} value is greater than its corresponding V_{HIGH} limit. 1 when V_{DD} is less than or equal to its corresponding V_{LOW} limit.

Internal Temperature Value/V_{DD} Value Register LSBs (Read-Only) [Address = 03h]

This 8-bit read-only register stores the two LSBs of the 10-bit temperature reading from the internal temperature sensor and the two LSBs of the 10-bit supply voltage reading.

Table 15. Internal Temperature/V_{DD} LSBs

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	V1	LSB	T1	LSB
N/A	N/A	N/A	N/A	0*	0*	0*	0*

*Default settings at power-up

Table 16.

Bit	Function
D0	LSB of Internal Temperature Value
D1	B1 of Internal Temperature Value
D2	LSB of V_{DD} Value
D3	B1 of V_{DD} Value

External Temperature Value and Analog Inputs 1 to 4 Register LSBs (Read-Only) [Address = 04h]

This is an 8-bit read-only register. Bits D2:D7 store the two LSBs of the analog inputs AIN2 to AIN4. Bits D0:D1 store the two LSBs of either the external temperature value or AIN1 input value. The type of input for D0 and D1 is selected by Bits C1:C2 of the Control Configuration Register 1.

Table 17. External Temperature and AIN1 to AIN4 LSBs

D7	D6	D5	D4	D3	D2	D1	D0
A4	$A4_{LSB}$	A3	$A3_{LSB}$	A2	$A2_{LSB}$	T/A	T/A_{LSB}
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

Table 18.

Bit	Function
D0	LSB of External Temperature Value or AIN1 Value
D1	Bit 1 of External Temperature Value or AIN1 Value
D2	LSB of AIN2 Value
D3	Bit 1 of AIN2 Value
D4	LSB of AIN3 Value
D5	Bit 1 of AIN3 Value
D6	LSB of AIN4 Value
D7	Bit 1 of AIN4 Value

V_{DD} Value Register MSBs (Read-Only) [Address = 6h]

This 8-bit read-only register stores the supply voltage value. The eight MSBs of the 10-bit value are stored in this register.

Table 19. V_{DD} Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
V9	V8	V7	V6	V5	V4	V3	V2
x*	x*	x*	x*	x*	x*	x*	x*

*Loaded with V_{DD} value after power-up.

Internal Temperature Value Register MSBs (Read-Only) [Address = 07h]

This 8-bit read-only register stores the internal temperature value from the internal temperature sensor in twos complement format. The eight MSBs of the 10-bit value are stored in this register.

Table 20. Internal Temperature Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T9	T8	T7	T6	T5	T4	T3	T2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

External Temperature Value or Analog Input AIN1 Register MSBs (Read-Only) [Address = 08h]

This 8-bit read-only register stores, if selected, the external temperature value or the analog input AIN1 value. Selection is done in the Control Configuration 1 register. The external temperature value is stored in twos complement format. The eight MSBs of the 10-bit value are stored in this register.

Table 21. External Temperature Value/Analog Inputs MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T/A9	T/A8	T/A7	T/A6	T/A5	T/A4	T/A3	T/A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

AIN2 Register MSBs (Read) [Address = 09h]

This 8-bit read register contains the eight MSBs of the AIN2 analog input voltage word. The value in this register is combined with Bits D2:3 of the external temperature value and Analog Inputs 1 to 4 register LSBs, Address 04h, to give the full 10-bit conversion result of the analog value on the AIN2 pin.

Table 22. AIN2 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

AIN3 Register MSBs (Read) [Address = 0Ah]

This 8-bit read register contains the eight MSBs of the AIN3 analog input voltage word. The value in this register is combined with Bits D4:5 of the external temperature value and Analog Inputs 1 to 4 register LSBs, Address 04h, to give the full 10-bit conversion result of the analog value on the AIN3 pin.

Table 23. AIN3 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

AIN4 Register MSBs (Read) [Address = 0Bh]

This 8-bit read register contains the eight MSBs of the AIN4 analog input voltage word. The value in this register is combined with Bits D6:7 of the external temperature value and Analog Inputs 1 to 4 register LSBs, Address 04h, to give the full 10-bit conversion result of the analog value on the AIN4 pin.

Table 24. AIN4 MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	A8	A7	A6	A5	A4	A3	A2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

DAC A Register (Read/Write) [Address = 11h]

This 8-bit read/write register contains the eight bits of the DAC A word. The value in this register is converted to an analog voltage on the V_{OUT}-A pin. On power-up, the voltage output on the V_{OUT}-A pin is 0 V.

Table 25. DAC A

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

DAC B Register (Read/Write) [Address = 13h]

This 8-bit read/write register contains the eight bits of the DAC B word. The value in this register is converted to an analog voltage on the V_{OUT}-B pin. On power-up, the voltage output on the V_{OUT}-B pin is 0 V.

Table 26. DAC B

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

DAC C Register (Read/Write) [Address = 15h]

This 8-bit read/write register contains the eight bits of the DAC C word. The value in this register is converted to an analog voltage on the V_{OUT}-C pin. On power-up, the voltage output on the V_{OUT}-C pin is 0 V.

Table 27. DAC C

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

DAC D Register (Read/Write) [Address = 17h]

This 8-bit read/write register contains the eight bits of the DAC D word. The value in this register is converted to an analog voltage on the V_{OUT}-D pin. On power-up, the voltage output on the V_{OUT}-D pin is 0 V.

Table 28. DAC D

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

Control Configuration 1 Register (Read/Write) [Address = 18h]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7518.

Table 29. Control Configuration 1

D7	D6	D5	D4	D3	D2	D1	D0
PD	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

Table 30.

Bit	Function
C0	This bit enables/disables conversions in round robin and single-channel mode. ADT7518 powers up in round robin mode but monitoring is not initiated until this bit is set. The default = 0. 0 = Stop monitoring. 1 = Start monitoring.
C2:C1	Selects between the two different analog inputs on Pins 7 and 8. ADT7518 powers up with AIN1 and AIN2 selected. 00 = AIN1 and AIN2 selected. 01 = Undefined. 10 = External TDM selected. 11 = Undefined.
C3	Selects between digital (LDAC) and analog inputs (AIN3) on Pin 9. When AIN3 is selected, Bit C3 of the Control Configuration 3 register is masked and has no effect until LDAC is selected as the input on Pin 9. 0 = LDAC selected. 1 = AIN3 selected.
C4	Reserved. Write 0 only.
C5	0 = Enable INT/$\overline{\text{INT}}$ output. 1 = Disable INT/$\overline{\text{INT}}$ output.
C6	Configures INT/$\overline{\text{INT}}$ output polarity. 0 = Active low. 1 = Active high.
PD	Power-Down Bit. Setting this bit to 1 puts the ADT7518 into standby mode. In this mode, both ADC and DACs are fully powered down, but the serial interface is still operational. To power up the part again, just write 0 to this bit.

Control Configuration 2 Register (Read/Write) [Address = 19h]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7518.

Table 31. Control Configuration 2

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Table 32.

Bit	Function
C2:0	In single-channel mode, these bits select between V_{DD}, the internal temperature sensor, external temperature sensor/AIN1, AIN2, AIN3, and AIN4 for conversion. The default is V_{DD}. 000 = V_{DD}. 001 = Internal temperature sensor. 010 = External temperature sensor/AIN1. (Bits C1:C2 of the Control Configuration 1 register affect this selection). 011 = AIN2. 100 = AIN3. 101 = AIN4. 110–111 = Reserved.
C3	Reserved.
C4	Selects between single-channel and round robin conversion cycle. The default is round robin. 0 = Round robin. 1 = Single channel.
C5	Default condition is to average every measurement on all channels 16 times. This bit disables this averaging. Channels affected are temperature, analog inputs, and V_{DD}. 0 = Enable averaging. 1 = Disable averaging.
C6	SMBus timeout on the serial clock puts a 25 ms limit on the pulse width of the clock, ensuring that a fault on the master SCL does not lock up the SDA line. 0 = Disable SMBus timeout. 1 = Enable SMBus timeout.
C7	Software Reset. Setting this bit to 1 causes a software reset. All registers and DAC outputs will reset to their default settings.

Control Configuration 3 Register (Read/Write) [Address = 1Ah]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7518.

Table 33. Control Configuration 3

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up

Table 34.

Bit	Function
C0	Selects between fast and slow ADC conversion speeds. 0 = ADC clock at 1.4 kHz. 1 = ADC clock at 22.5 kHz. D+ and D– analog filters are disabled.
C2:1	Reserved. Write 0 only.
C3	0 = $\overline{\text{LDAC}}$ pin controls updating of DAC outputs. 1 = DAC configuration register and LDAC configuration register control updating of DAC outputs.
C4	Selects the ADC reference to be either internal V_{REF} or V_{DD} for analog inputs. 0 = Internal V_{REF}. 1 = V_{DD}.
C5	Setting this bit selects DAC A voltage output to be proportional to the internal temperature measurement.
C6	Setting this bit selects DAC B voltage output to be proportional to the external temperature measurement.
C7	Reserved. Write 0 only.

DAC Configuration Register (Read/Write) [Address = 1Bh]

This configuration register is an 8-bit read/write register that is used to control the output ranges of all four DACs and also to control the loading of the DAC registers if the $\overline{\text{LDAC}}$ pin is disabled (Bit C3 = 1, Control Configuration 3 register).

Table 35. DAC Configuration

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Table 36.

Bit	Function
D0	Selects the output range of DAC A. 0 = 0 V to V_{REF}. 1 = 0 V to $2V_{REF}$.
D1	Selects the output range of DAC B. 0 = 0 V to V_{REF}. 1 = 0 V to $2V_{REF}$.
D2	Selects the output range of DAC C. 0 = 0 V to V_{REF}. 1 = 0 V to $2V_{REF}$.
D3	Selects the output range of DAC D. 0 = 0 V to V_{REF}. 1 = 0 V to $2V_{REF}$.
D5:D4	00 = A write to any DAC register generates LDAC command that updates that DAC only. 01 = A write to DAC B or DAC D register generates LDAC command that updates DACs A, B or DACs C, D, respectively. 10 = A write to DAC D register generates LDAC command that updates all four DACs. 11 = LDAC command generated from LDAC register.
D6:D7	Reserved. Write 0s only.

LDAC Configuration Register (Write-Only) [Address = 1Ch]

This configuration register is an 8-bit write register that is used to control the updating of the quad DAC outputs if the $\overline{\text{LDAC}}$ pin is disabled and Bits D4:D5 of the DAC configuration register are both set to 1. Also selects either the internal or external V_{REF} for all four DACs. Bits D0:D3 in this register are self-clearing, i.e., reading back from this register will always give 0s for these bits.

Table 37. LDAC Configuration

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Table 38.

Bit	Function
D0	Writing a 1 to this bit will generate the LDAC command to update DAC A output only.
D1	Writing a 1 to this bit will generate the LDAC command to update DAC B output only.
D2	Writing a 1 to this bit will generate the LDAC command to update DAC C output only.
D3	Writing a 1 to this bit will generate the LDAC command to update DAC D output only.
D4	Selects either internal V_{REF} or external V_{REF} for DACs A and B. 0 = External V_{REF} 1 = Internal V_{REF}.
D5	Selects either internal V_{REF} or external V_{REF} for DACs C and D. 0 = External V_{REF} 1 = Internal V_{REF}
D6:D7	Reserved. Write 0s only.

Interrupt Mask 1 Register (Read/Write) [Address = 1Dh]

This mask register is an 8-bit read/write register that can be used to mask any interrupts that can cause the INT/$\overline{\text{INT}}$ pin to go active.

Table 39. Interrupt Mask 1

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Table 40.

Bit	Function
D0	0 = Enable internal T_{HIGH} interrupt. 1 = Disable internal T_{HIGH} interrupt.
D1	0 = Enable internal T_{LOW} interrupt. 1 = Disable internal T_{LOW} interrupt.
D2	0 = Enable external T_{HIGH} interrupt or AIN1 interrupt. 1 = Disable external T_{HIGH} interrupt or AIN1 interrupt.
D3	0 = Enable external T_{LOW} interrupt. 1 = Disable external T_{LOW} interrupt.
D4	0 = Enable external temperature fault interrupt.. 1 = Disable external temperature fault interrupt.
D5	0 = Enable AIN2 interrupt. 1 = Disable AIN2 interrupt.
D6	0 = Enable AIN3 interrupt. 1 = Disable AIN3 interrupt.
D7	0 = Enable AIN4 interrupt. 1 = Disable AIN4 interrupt.

Interrupt Mask 2 Register (Read/Write) [Address = 1Eh]

This mask register is an 8-bit read/write register that can be used to mask any interrupts that can cause the INT/$\overline{\text{INT}}$ pin to go active.

Table 41. Interrupt Mask 2

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Table 42.

Bit	Function
D0:D3	Reserved. Write 0s only.
D4	0 = Enable V_{DD} interrupts. 1 = Disable V_{DD} interrupts.
D5:D7	Reserved. Write 0s only.

Internal Temperature Offset Register (Read/Write) [Address = 1Fh]

This register contains the offset value for the internal temperature channel. A twos complement number can be written to this register which is then added to the measured result before it is stored or compared to limits. In this way, a one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. Because it is an 8-bit register, the temperature resolution is 1°C.

Table 43. Internal Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

External Temperature Offset Register (Read/Write) [Address = 20h]

This register contains the offset value for the external temperature channel. A twos complement number can be written to this register, which is then added to the measured result before it is stored or compared to limits. In this way, a one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. Because it is an 8-bit register, the temperature resolution is 1°C.

Table 44. External Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Internal Analog Temperature Offset Register (Read/Write) [Address = 21h]

This register contains the offset value for the internal thermal voltage output. A twos complement number can be written to this register, which is then added to the measured result before it is converted by DAC A. Varying the value in this register has the effect of varying the temperature span. For example, the output voltage can represent a temperature span of –128°C to +127°C or even 0°C to +127°C. In essence, this register changes the position of 0 V on the temperature scale. Temperatures other than –128°C to +127°C will produce an upper deadband on the DAC A output. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is –40°C.

Table 45. Internal Analog Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	1*	1*	0*	0*	0*

* Default settings at power-up

External Analog Temperature Offset Register (Read/Write) [Address = 22h]

This register contains the offset value for the external thermal voltage output. A twos complement number can be written to this register which is then added to the measured result before it is converted by DAC B. Varying the value in this register has the effect of varying the temperature span. For example, the output voltage can represent a temperature span of –128°C to +127°C or even 0°C to +127°C. In essence, this register changes the position of 0 V on the temperature scale. Temperatures other than –128°C to +127°C will produce an upper deadband on the DAC B output. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is –40°C.

Table 46. External Analog Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	1*	1*	0*	0*	0*

* Default settings at power-up

V_{DD} V_{HIGH} Limit Register (Read/Write) [Address = 23h]

This limit register is an 8-bit read/write register that stores the V_{DD} upper limit, which will cause an interrupt and activate the INT/$\overline{\text{INT}}$ output (if enabled). For this to happen, the measured V_{DD} value has to be greater than the value in this register. The default value is 5.46 V.

Table 47. V_{DD} V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	0*	1*	1*	1*

* Default settings at power-up

V_{DD} V_{LOW} Limit Register (Read/Write) [Address = 24h]

This limit register is an 8-bit read/write register that stores the V_{DD} lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured V_{DD} value has to be less than or equal to the value in this register. The default value is 2.7 V.

Table 48. V_{DD} V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	0*	1*	0*

* Default settings at power-up

Internal T_{HIGH} Limit Register (Read/Write) [Address = 25h]

This limit register is an 8-bit read/write register that stores the twos complement of the internal temperature upper limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured internal temperature value has to be greater than the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is +100°C.

Table 49. Internal T_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	1*	0*	0*

* Default settings at power-up

Internal T_{LOW} Limit Register (Read/Write) [Address = 26h]

This limit register is an 8-bit read/write register that stores the twos complement of the internal temperature lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured internal temperature value has to be more negative than or equal to the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is –55°C.

Table 50. Internal T_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	1*	0*	0*	1*

* Default settings at power-up

External T_{HIGH}/AIN1 V_{HIGH} Limit Register (Read/Write) [Address = 27h]

If Pins 7 and 8 are configured for the external temperature sensor, this limit register is an 8-bit read/write register that stores the twos complement of the external temperature upper limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured external temperature value has to be greater than the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is –1°C.

If Pins 7 and 8 are configured for AIN1 and AIN2 inputs, this limit register is an 8-bit read/write register that stores the AIN1 input upper limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN1 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. Because the power-up default settings for Pins 7 and 8 are AIN1 and AIN2 inputs, the default value for this limit register is full-scale voltage.

Table 51. AIN1 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

* Default settings at power-up

External T_{LOW}/AIN1 V_{LOW} Limit Register (Read/Write) [Address = 28h]

If Pins 7 and 8 are configured for the external temperature sensor, this limit register is an 8-bit read/write register that stores the twos complement of the external temperature lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured external temperature value has to be more negative than or equal to the value in this register. Because it is an 8-bit register, the temperature resolution is 1°C. The default value is 0°C.

If Pins 7 and 8 are configured for AIN1 and AIN2 inputs, this limit register is an 8-bit read/write register that stores the AIN1 input lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN1 value has to be less than or equal to the value in this register. As it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. Because the power-up default settings for Pins 7 and 8 are AIN1 and AIN2 inputs, the default value for this limit register is 0 V.

Table 52. AIN1 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

AIN2 V_{HIGH} Limit Register (Read/Write) [Address = 2Bh]

This limit register is an 8-bit read/write register that stores the AIN2 input upper limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN2 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 53. AIN2 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

* Default settings at power-up

AIN2 V_{LOW} Limit Register (Read/Write) [Address = 2Ch]

This limit register is an 8-bit read/write register that stores the AIN2 input lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN2 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 54. AIN2 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

AIN3 V_{HIGH} Limit Register (Read/Write) [Address = 2Dh]

This limit register is an 8-bit read/write register that stores the AIN3 input upper limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN3 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 55. AIN3 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

* Default settings at power-up

AIN3 V_{LOW} Limit Register (Read/Write) [Address = 2Eh]

This limit register is an 8-bit read/write register that stores the AIN3 input lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN3 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 56. AIN3 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

AIN4 V_{HIGH} Limit Register (Read/Write) [Address = 2Fh]

This limit register is an 8-bit read/write register that stores the AIN4 input upper limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN4 value has to be greater than the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is full-scale voltage.

Table 57. AIN4 V_{HIGH} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

* Default settings at power-up

AIN4 V_{LOW} Limit Register (Read/Write) [Address = 30h]

This limit register is an 8-bit read/write register that stores the AIN4 input lower limit, which will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured AIN4 value has to be less than or equal to the value in this register. Because it is an 8-bit register, the resolution is four times less than the resolution of the 10-bit ADC. The default value is 0 V.

Table 58. AIN4 V_{LOW} Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

* Default settings at power-up

Device ID Register (Read-Only) [Address = 4Dh]

This 8-bit read-only register contains a device identifier byte: ADT7518 = 0Bh.

Manufacturer's ID Register (Read-Only) [Address = 4Eh]

This register contains the manufacturer's identification number. ADI's ID number is 41h.

Silicon Revision Register (Read-Only) [Address = 4Fh]

This register is divided into four LSBs representing the stepping and the four MSBs representing the version. The stepping contains the manufacturer's code for minor revisions or steppings to the silicon. The version is the ADT7518 version number.

SPI Lock Status Register (Read-Only) [Address = 7Fh]

Bit D0 (LSB) of this read-only register indicates whether or not the SPI interface is locked. Writing to this register will cause the device to malfunction. The default value is 00h.

0 = I^2C interface.
1 = SPI interface selected and locked.

SERIAL INTERFACE

There are two serial interfaces that can be used on this part: I^2C and SPI. The device will power up with the serial interface in I^2C mode, but it is not locked into this mode. To stay in I^2C mode, it is recommended that the user tie the $\overline{CS}$ line to either V_{CC} or GND. It is not possible to lock the I^2C mode, but it is possible to select and lock the SPI mode.

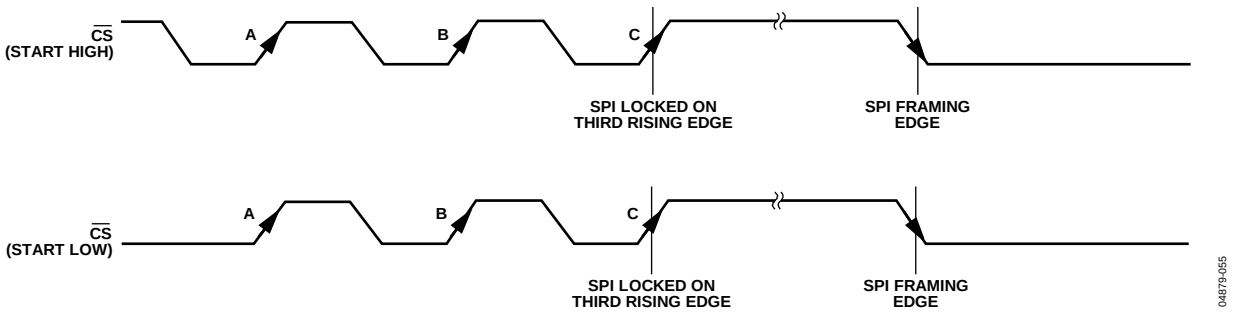


Figure 53. Serial Interface—Selecting and Locking SPI Protocol

To select and lock the interface into the SPI mode, a number of pulses must be sent down the $\overline{CS}$ line (Pin 4). The following section describes how this is done.

Once the SPI communication protocol has been locked in, it cannot be unlocked while the device is still powered up. Bit D0 of the SPI lock status register (Address 7Fh) is set to 1 when a successful SPI interface lock has been accomplished. To reset the serial interface, the user must power down the part and power it up again. A software reset does not reset the serial interface.

Serial Interface Selection

The $\overline{CS}$ line controls the selection between I²C and SPI. Figure 53 shows the selection process necessary to lock the SPI interface mode.

To communicate to the ADT7518 using the SPI protocol, send three pulses down the $\overline{CS}$ line as shown in Figure 53. On the third rising edge (marked as C in Figure 53), the part selects and locks the SPI interface. The user is now limited to communicating to the device using the SPI protocol.

As per most SPI standards, the CS line must be low during every SPI communication to the ADT7518 and high all other times. Typical examples of how to connect the dual interface as I²C or SPI is shown in Figure 54 and Figure 55. The following sections describe in detail how to use the I²C and SPI protocols associated with the ADT7518.

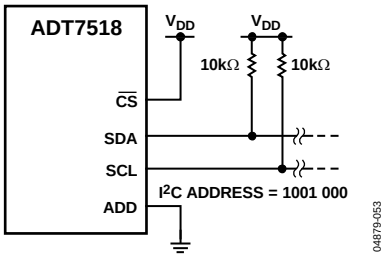


Figure 54. Typical I²C Interface Connection

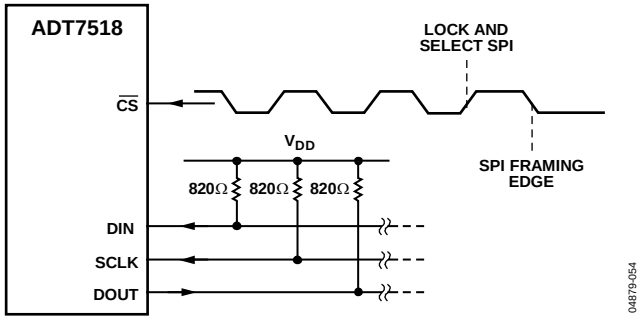


Figure 55. Typical SPI Interface Connection

I²C Serial Interface

Like all I²C-compatible devices, the ADT7518 has a 7-bit serial address. The four MSBs of this address for the ADT7518 are set to 1001. The three LSBs are set by Pin 11, ADD. The ADD pin can be configured three ways to give three different address options: low, floating, and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the address 1001 010, and setting it high gives the address 1001 011. The recommended pull-up resistor value is 10 kΩ.

There is an enable/disable bit for the SMBus timeout. When this is enabled, the SMBus will time out after 25 ms of no activity. To enable it, set Bit 6 of the Control Configuration 2 register. The power-on default is with the SMBus timeout disabled.

The ADT7518 supports SMBus packet error checking (PEC), but its use is optional. It is triggered by supplying the extra clocks for the PEC byte. The PEC is calculated using CRC-8. The frame clock sequence (FCS) conforms to CRC-8 by the polynominal

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult the SMBus specification (*www.smbus.org*) for more information.

The serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0 the master will write to the slave device. If the R/$\overline{W}$ bit is 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low to high transition when the clock is high may be interpreted as a stop signal.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master will pull the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device will pull the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

The I^2C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. This is the SCL cycle directly after the device has seen its own I^2C serial bus address. Any subsequent changes on this pin will have no effect on the I^2C serial bus address.

Writing to the ADT7518

Depending on the register being written to, there are two different writes for the ADT7518. It is not possible to do a block write to this part, i.e., no I^2C autoincrement.

Writing to the Address Pointer Register for a Subsequent Read

To read data from a particular register, the address pointer register must contain the address of that register. If it does not, the correct address must be written to the address pointer register by performing a single-byte write operation, as shown in Figure 56. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.

Writing Data to a Register

All registers are 8-bit registers, so only one byte of data can be written to each register. Writing a single byte of data to one of these read/write registers consists of the serial bus address, the data register address written to the address pointer register, followed by the data byte written to the selected data register. This is illustrated in Figure 57. To write to a different register, another start or repeated start is required. If more than one byte of data is sent in one communication operation, the addressed register will repeatedly load until the last data byte is sent.

Reading Data from the ADT7518

Reading data from the ADT7518 is done in a 1-byte operation. Reading back the contents of a register is shown in Figure 58. The register address had previously been set up by a single-byte write operation to the address pointer register. To read from another register, write to the address pointer register again to set up the relevant register address. Thus, block reads are not possible, i.e., no I^2C autoincrement.

SPI Serial Interface

The SPI serial interface of the ADT7518 consists of four wires: $\overline{CS}$, SCLK, DIN, and DOUT. The $\overline{CS}$ line is used to select the device when more than one device is connected to the serial clock and data lines. The $\overline{CS}$ line is also used to distinguish between any two separate serial communications (see Figure 63 for a graphical explanation). The SCLK line is used to clock data in and out of the part. The D_{IN} line is used to write to the registers, and the DOUT line is used to read data back from the registers. The recommended pull-up resistor value is between 500 Ω and 820 Ω.

The part operates in slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations, read and write. Command words are used to distinguish read operations from write operations. These command words are given in Table 59. Address autoincrement is possible in SPI mode.

Table 59. SPI Command Words

Write	Read
90h (1001 0000)	91h (1001 0001)

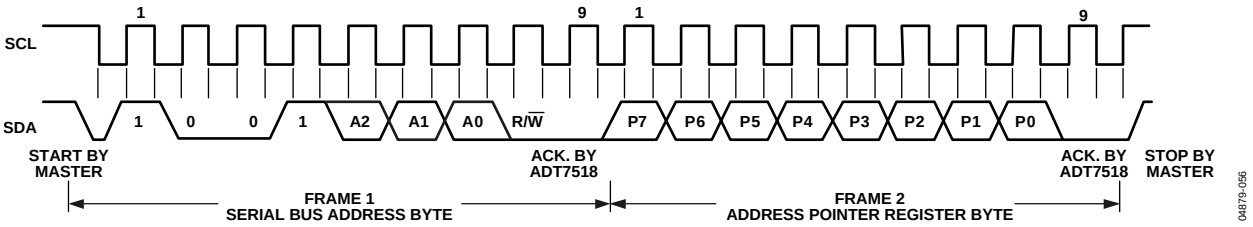


Figure 56. I²C—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation

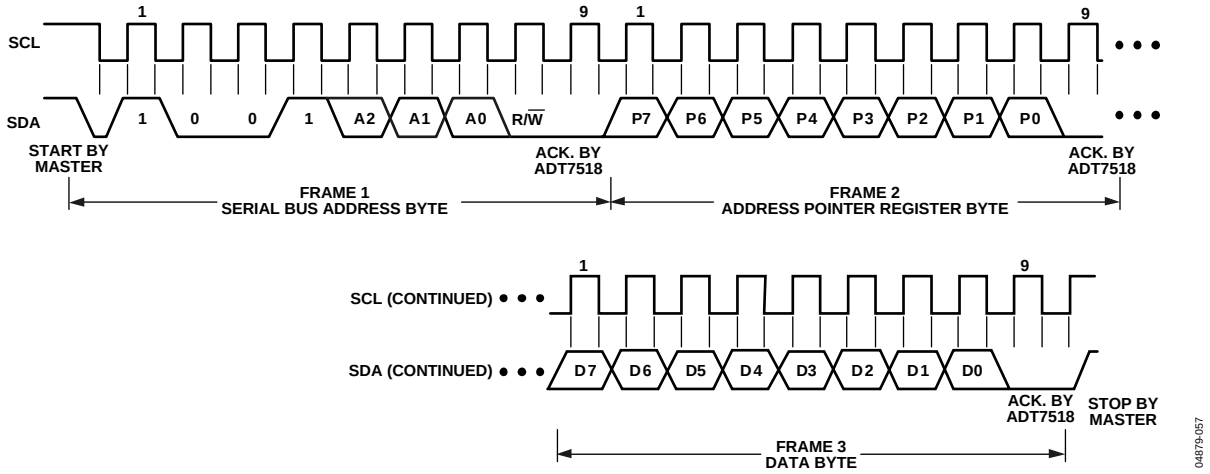


Figure 57. I²C—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

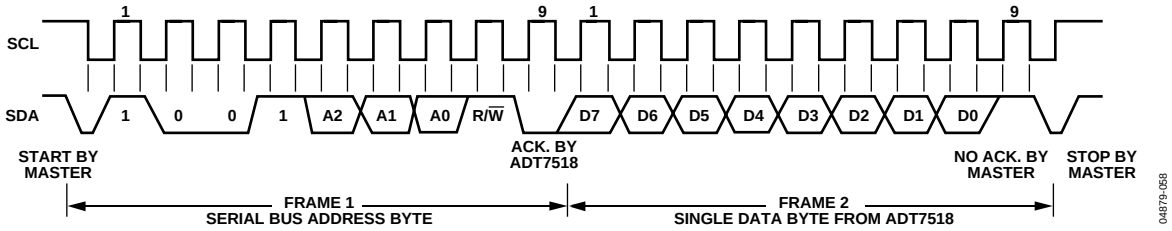


Figure 58. I²C—Reading a Single Byte of Data from a Selected Register

Write Operation

Figure 59 shows the timing diagram for a write operation to the ADT7518. Data is clocked into the registers on the rising edge of SCLK. When the $\overline{CS}$ line is high, the DIN and DOUT lines are in three-state mode. Only when the $\overline{CS}$ goes from a high to a low does the part accept any data on the DIN line. In SPI mode, the address pointer register is capable of autoincrementing to the next register in the register map without having to load the address pointer register each time. In Figure 59, the register address portion gives the first register that will be written to. Subsequent data bytes will be written into sequential writable registers. Thus, after each data byte has been written into a register, the address pointer register autoincrements its value to the next available register. The address pointer register will autoincrement from 00h to 3Fh and will loop back to start again at 00h when it reaches 3Fh.

Read Operation

Figure 60 to Figure 62 show the timing diagrams necessary to accomplish correct read operations. To read back from a register, first write to the address pointer register with the address of the register to be read from. This operation is shown in Figure 60. Figure 61 shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first eight clock cycles. During the following eight clock cycles, the data contained in the register selected by the address pointer register is output onto the D_{OUT} line. Data is output onto the D_{OUT} line on the falling edge of SCLK. Figure 62 shows the procedure when reading data from two sequential registers. Multiple data reads are possible in the SPI interface mode as the address pointer register is autoincremental. The address pointer register will autoincrement from 00h to 3Fh and will loop back to start again at 00h when it reaches 3Fh.

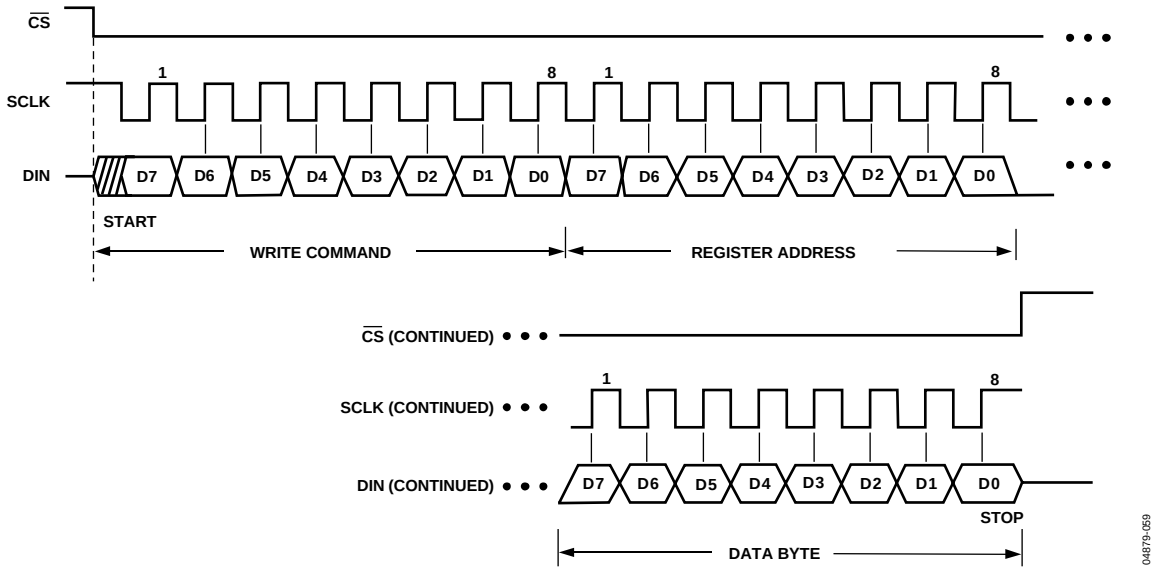


Figure 59. SPI—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

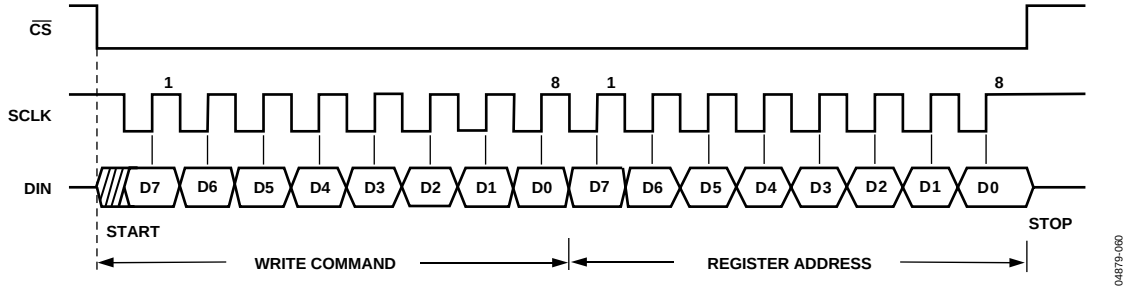


Figure 60. SPI—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation

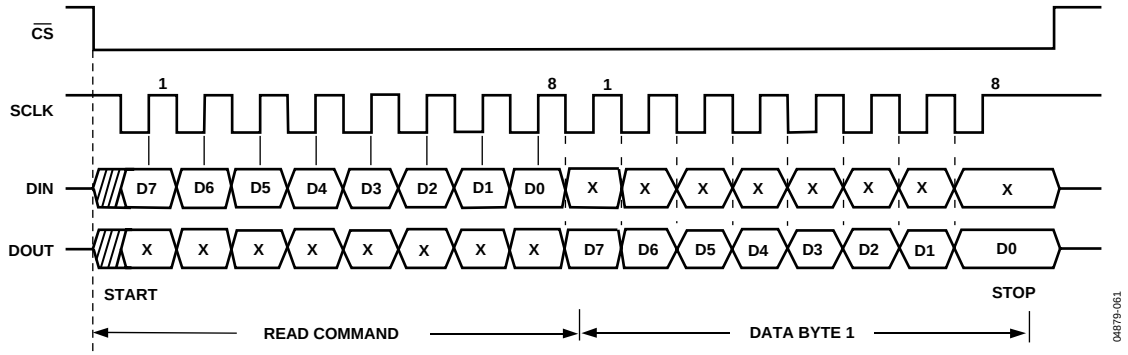


Figure 61. SPI—Reading a Single Byte of Data From a Selected Register

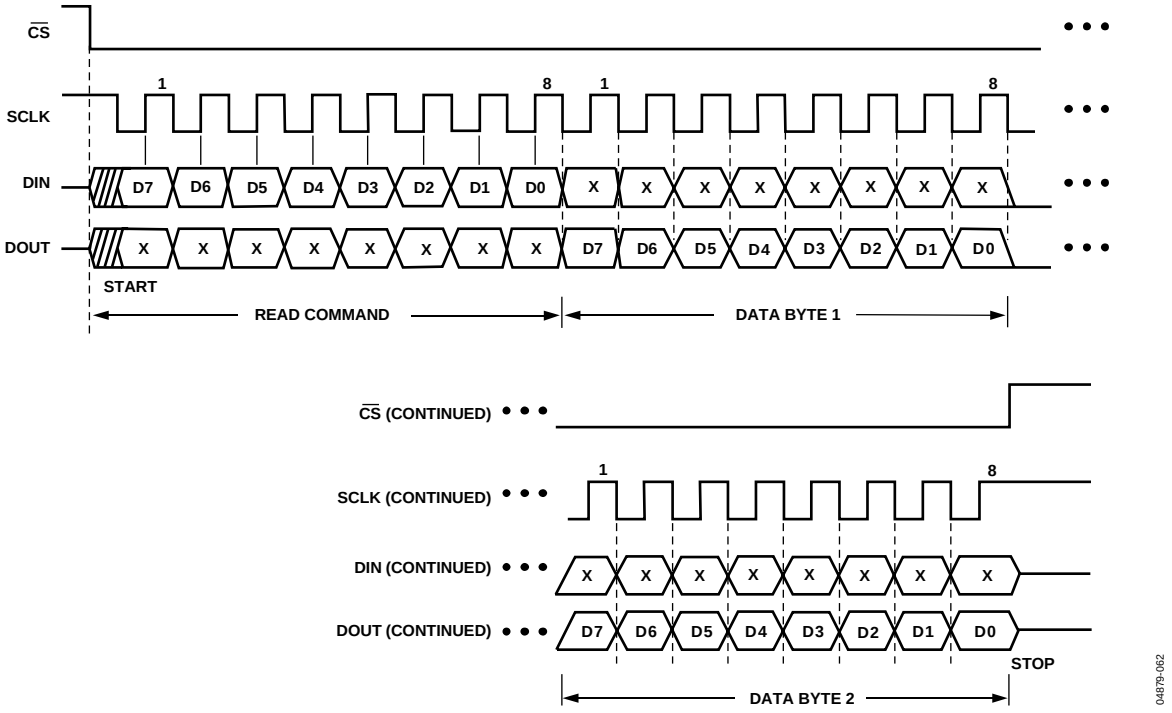


Figure 62. SPI—Reading Two Bytes of Data From Two Sequential Registers

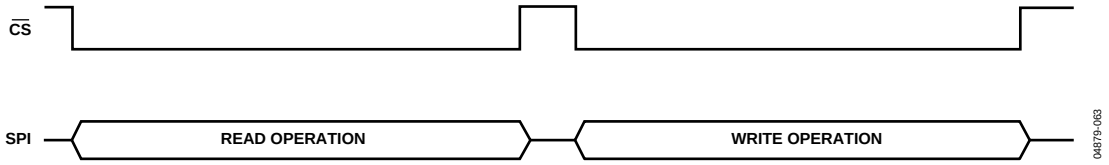


Figure 63. SPI—Correct Use of $\overline{CS}$ During SPI Communication

SMBus/SPI INT/$\overline{INT}$

The ADT7518 INT/$\overline{INT}$ output is an interrupt line for devices that want to trade their ability to master for an extra pin. It is a slave device and uses the SMBus/SPI INT/$\overline{INT}$ to signal the host device that it wants to talk to. The SMBus/SPI INT/$\overline{INT}$ on the ADT7518 is used as an over/under limit indicator.

The INT/$\overline{INT}$ pin has an open-drain configuration that allows the outputs of several devices to be wired-AND'ed together when the INT/$\overline{INT}$ pin is active low. Use C6 of the Control Config-uration 1 register to set the active polarity of the INT/$\overline{INT}$ out-put. The power-up default is active low. The INT/$\overline{INT}$ output can be disabled or enabled by setting C5 of the Control Config-uration 1 register to 1 or 0, respectively.

The INT/$\overline{INT}$ output becomes active when either the internal temperature value, the external temperature value, V_{DD} value, or any of the AIN input values exceed the values in their corresponding T_{HIGH}/V_{HIGH} or T_{LOW}/V_{LOW} registers. The INT/$\overline{INT}$ output goes inactive again when a conversion result has the measured value back within the trip limits and when the status register associated with the out-of-limit event is read. The two interrupt status registers show which event caused the INT/$\overline{INT}$ pin to go active.

The INT/$\overline{INT}$ output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD}, provided the maximum voltage rating of the INT/$\overline{INT}$ output pin is not exceeded. The value of the pull-up resistor depends on the application but should be large enough to avoid excessive sink currents at the INT/$\overline{INT}$ output, which can heat the chip and affect the temperature reading.

SMBUS ALERT RESPONSE

The INT/$\overline{INT}$ pin behaves the same way as an SMBus alert pin when the SMBus/I²C interface is selected. It is an open-drain output and requires a pull-up to V_{DD}. Several INT/$\overline{INT}$ outputs can be wire-AND'ed together, so that the common line will go low if one or more of the INT/$\overline{INT}$ outputs goes low. The polarity of the INT/$\overline{INT}$ pin must be set active low for a number of outputs to be wire-AND'ed together.

The INT/$\overline{\text{INT}}$ output can operate as an $\overline{\text{SMBALERT}}$ function. Slave devices on the SMBus cannot normally signal to the master that they want to talk, but the $\overline{\text{SMBALERT}}$ function allows them to do so. $\overline{\text{SMBALERT}}$ is used in conjunction with the SMBus general call address.

One or more INT/$\overline{\text{INT}}$ outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. When the $\overline{\text{SMBALERT}}$ line is pulled low by one of the devices, the following procedure occurs, as shown in Figure 64.

1. $\overline{\text{SMBALERT}}$ pulled low.
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The devices whose INT/$\overline{\text{INT}}$ output is low responds to the alert response address and the master reads its device address. As the device address is seven bits long, an LSB of 1 is added. The address of the device is now known and it can be interrogated in the usual way.
4. If more than one device's INT/$\overline{\text{INT}}$ output is low, the one with the lowest device address will have priority in accordance with normal SMBus specifications.
5. Once the ADT7518 has responded to the alert response address, it will reset its INT/$\overline{\text{INT}}$ output, provided that the condition that caused the out-of-limit event no longer exists and that the status register associated with the out-of-limit event is read. If the $\overline{\text{SMBALERT}}$ line remains low, the master will send the ARA again. It will continue to do this until all devices whose $\overline{\text{SMBALERT}}$ outputs were low have responded.

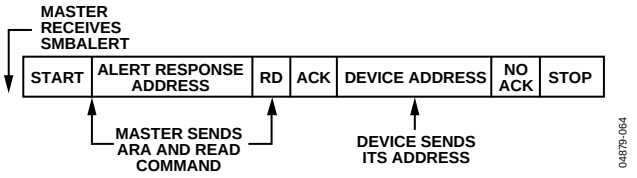


Figure 64. INT/$\overline{\text{INT}}$ Responds to $\overline{\text{SMBALERT}}$ ARA

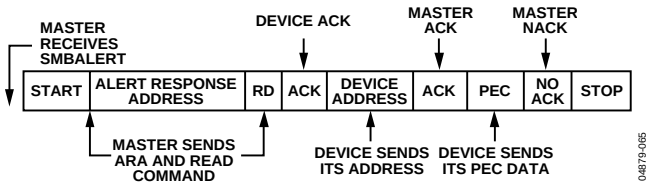
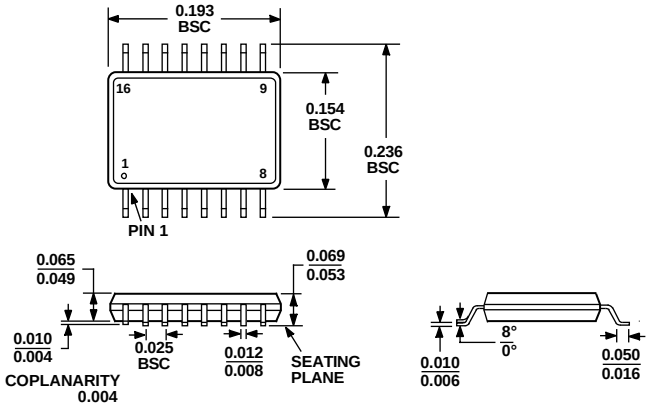


Figure 65. INT/$\overline{\text{INT}}$ Responds to $\overline{\text{SMBALERT}}$ ARA With Packet Error Checking (PEC)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137AB

Figure 66. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions in Inches

ORDERING GUIDE

Model	Temperature Range	DAC Resolution	Package Description	Package Option	Minimum Quantities/Reel
ADT7518ARQ	–40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	N/A
ADT7518ARQ-REEL	–40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	2,500
ADT7518ARQ-REEL7	–40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	1,000
ADT7518ARQZ[1]	–40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	N/A
ADT7518ARQZ-REEL[1]	–40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	2,500
ADT7518ARQZ-REEL7[1]	–40°C to +120°C	8 Bits	16-Lead QSOP	RQ-16	1,000

[1] Z = Pb-free part.

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